Application Stability of Fast Switching Planar SiC MOSFETs

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Alpha and Omega Semiconductor

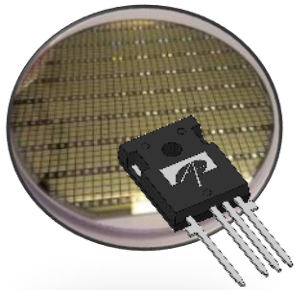
Bodo's Wide Bandgap Event 2024

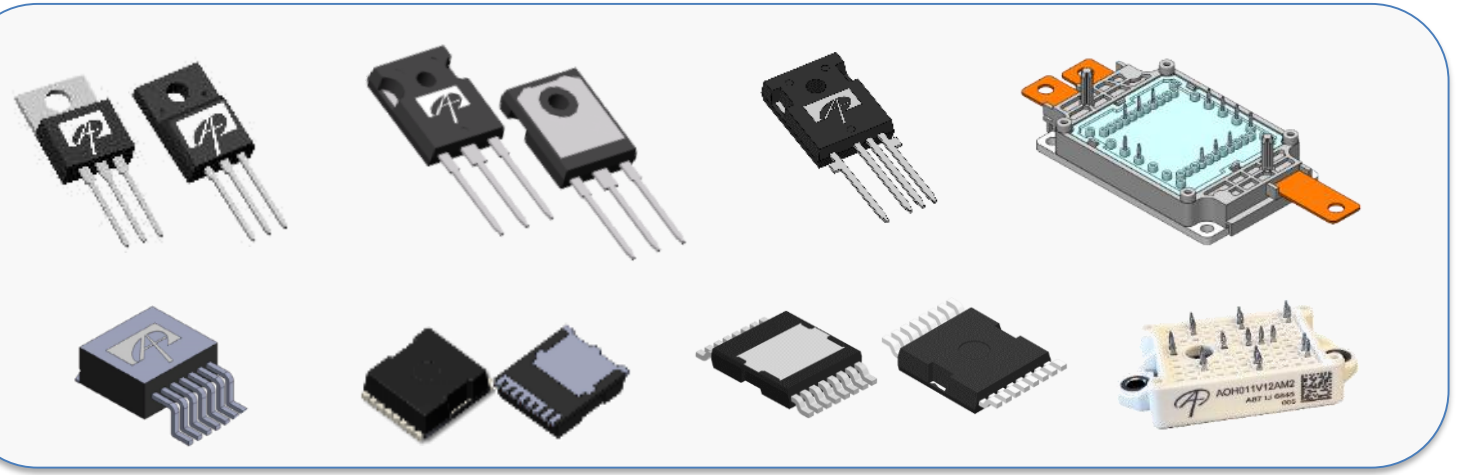
Making WBG Designs Happen

SiC

AOS / Silicon Carbide Introduction

- **Alpha and Omega Semiconductor (AOS)**
  - Headquarters: Sunnyvale, CA
  - Global Employees: 2500
  - 8” and 12” In-house IATF16949
  - Si Discrete Power Fabs
  - Si MOSFETs, IGBT, SJ-MOS, PIC, WBG
  - Leading 5th MOSFET supplier WW (2021)
  - 2 In-house IATF16949 discrete/module assy & test locations





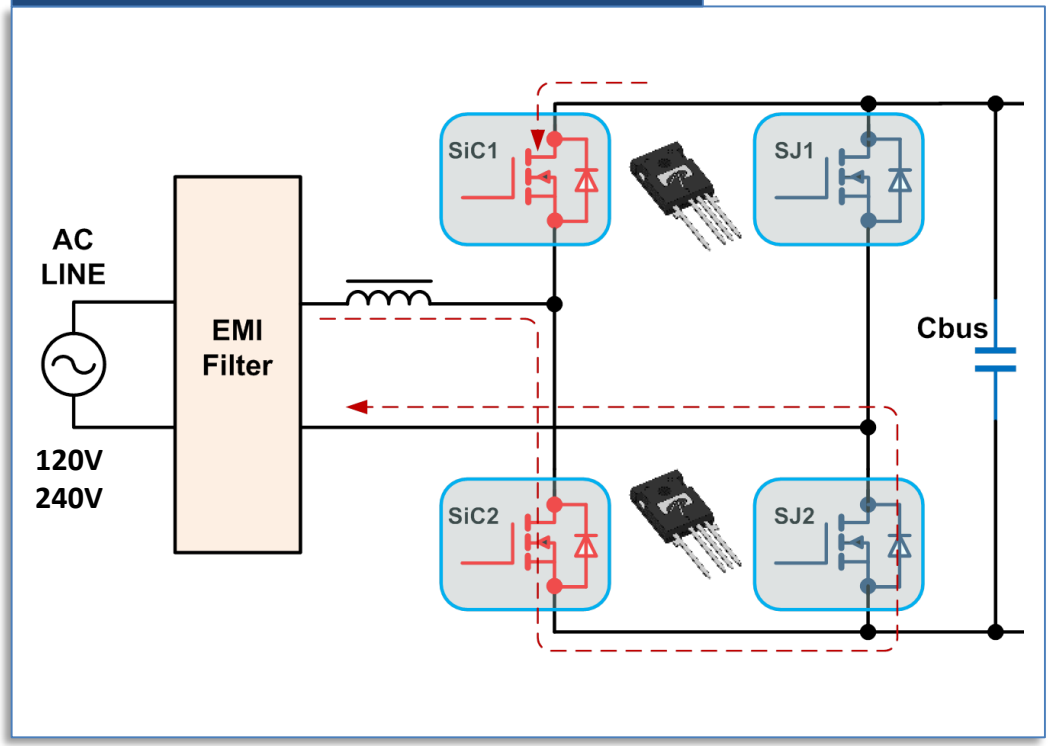
650V, 750V, 1200V, 1700V

15mΩ – 500mΩ

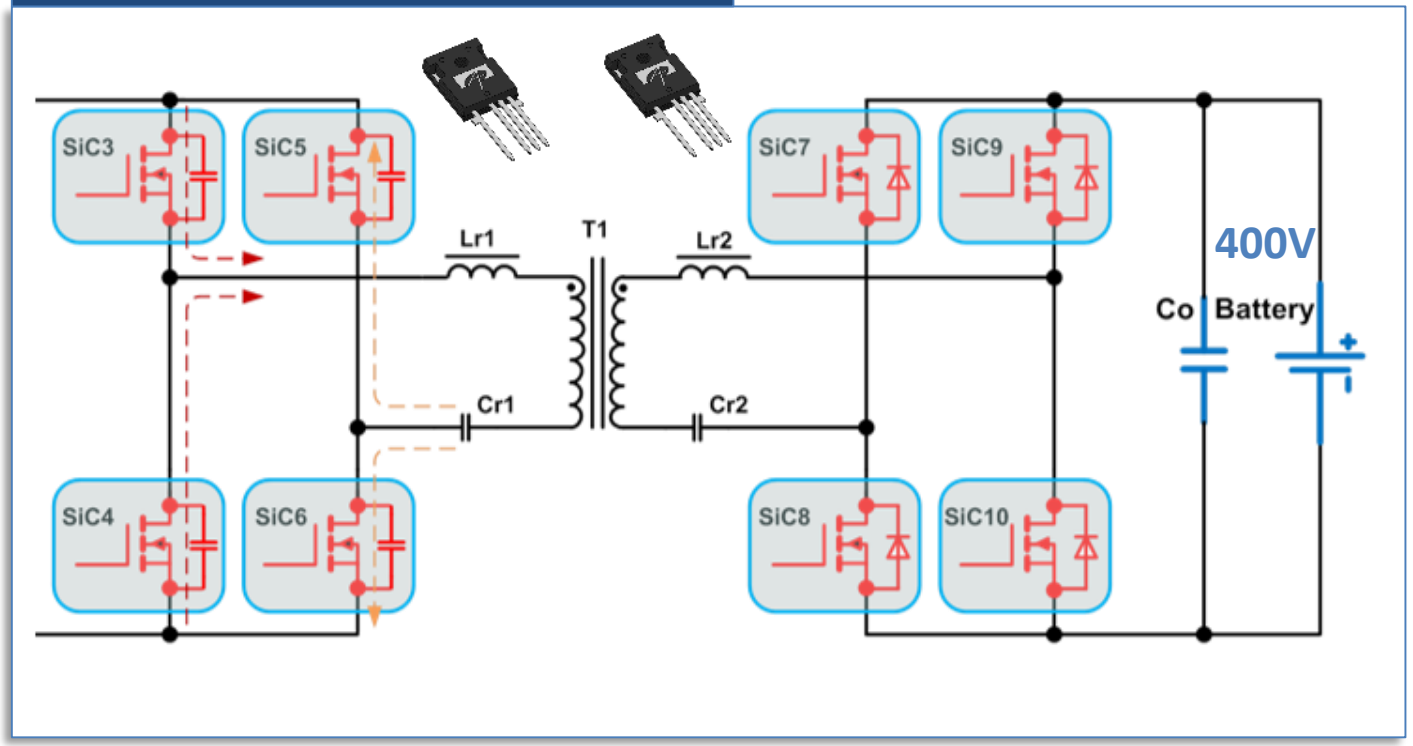
General SiC Applications

- **Industrial and Automotive Applications: Solar, Server/Telecom, Auto OBC - Inverter**

Hard Switching: Totem-Pole PFC



Resonant: CLLC, DAB, CLLLC, Etc.



High Efficiency Hard Switching Applications

Question: Can I switch a SiC MOSFET at $V_{GS,off}$=0V drive conditions?

High Efficiency Hard Switching Applications

Question: Can I switch a SiC MOSFET at $V_{GS,off}$=0V drive conditions?

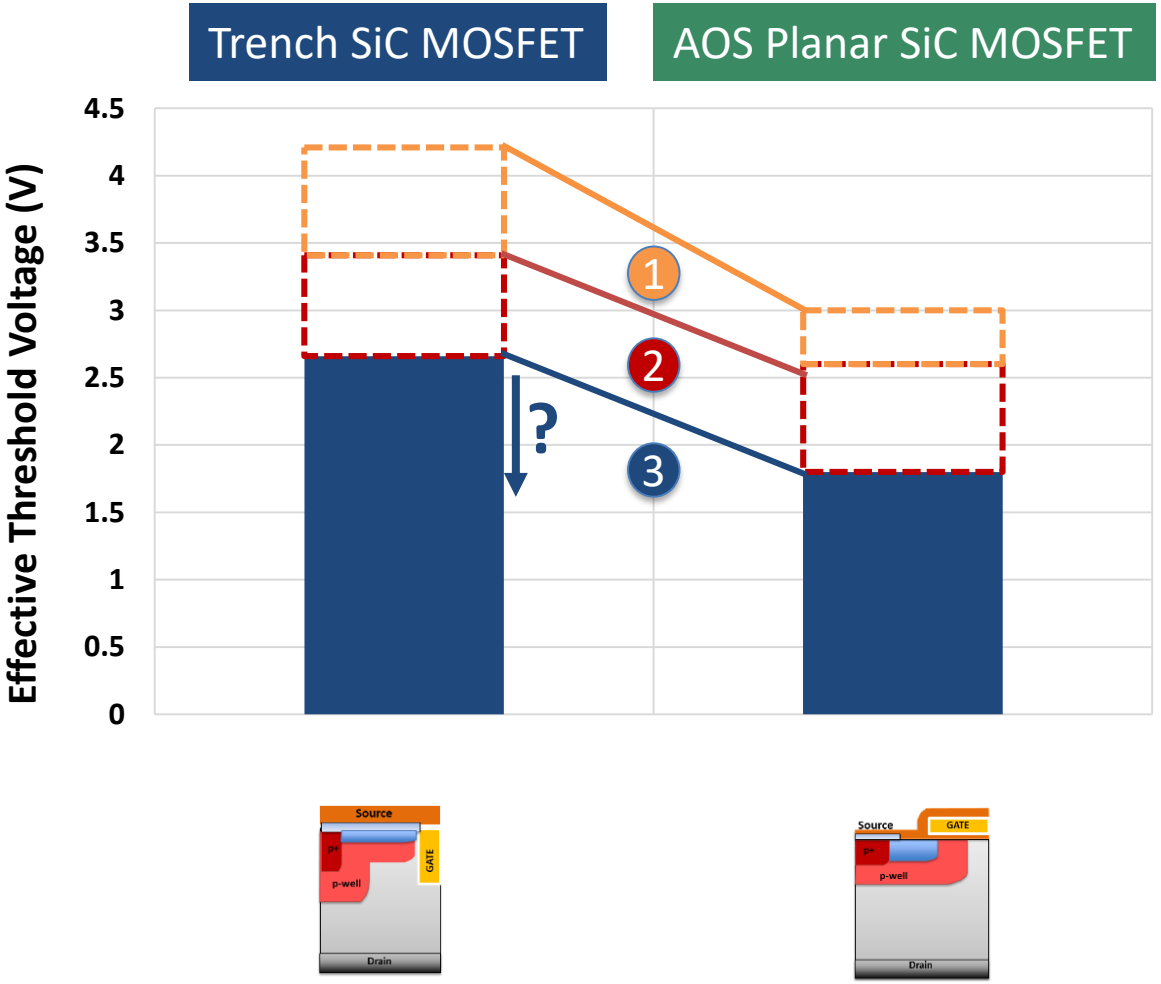
Answer: Maybe

Considerations:

- SiC MOSFET Characteristics
  - C_{GS}/C_{GD}
  - Threshold voltage
- Gate Driver
  - Miller clamp
- Circuit and Application Conditions
  - Hard Switching
  - Driving dV/dt
  - Gate/Source loop inductances
  - Layout design

What is Threshold Voltage in Application?

- **In Practice, Datasheet Vth can be different**



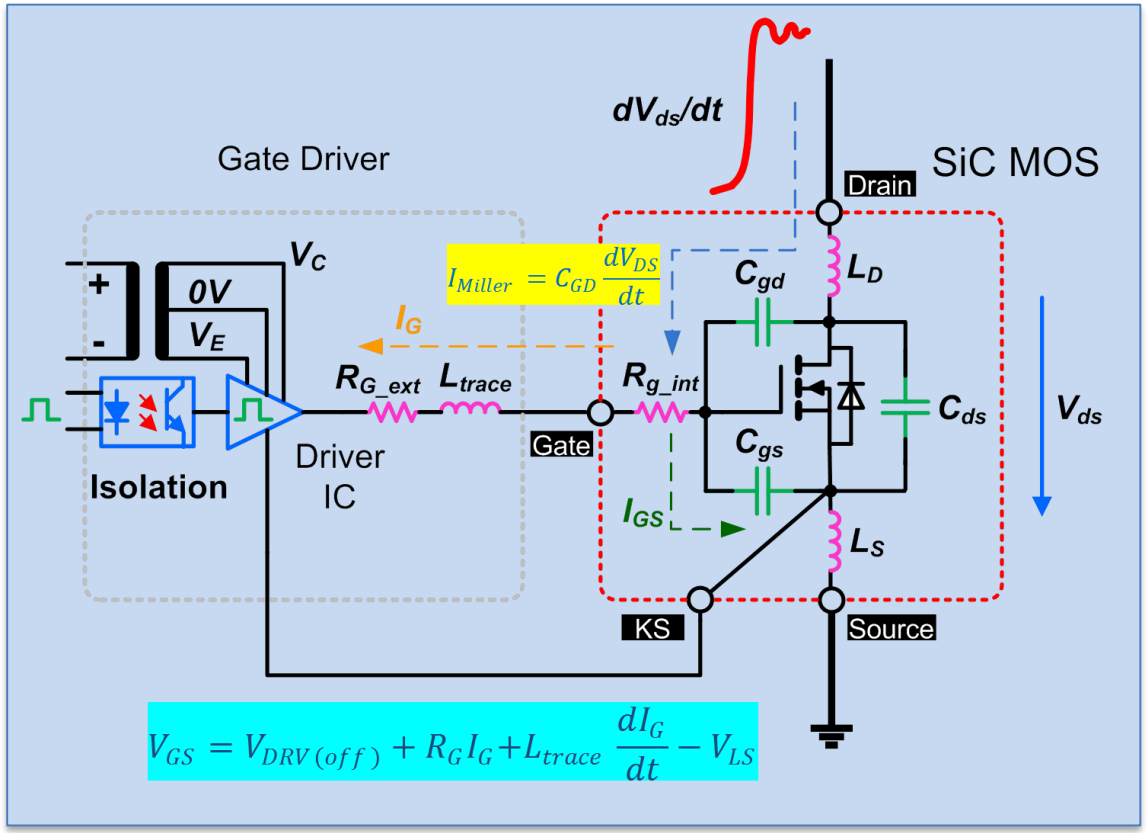
1. ***DIBL affect static Vth at high voltage***
   - Drain bias reduces channel barrier
   - Less VGS required to turn on device

2. ***Vth reduces at high temperature***
   - Simple device physics
   - Lowering of barrier with T

3. ***Switching reduces effective Vth at high dV/dt***
   - Classic shoot-through circuit dynamics
   - Internal R_G, C_{GS}, C_{GD}, starting V_{TH}

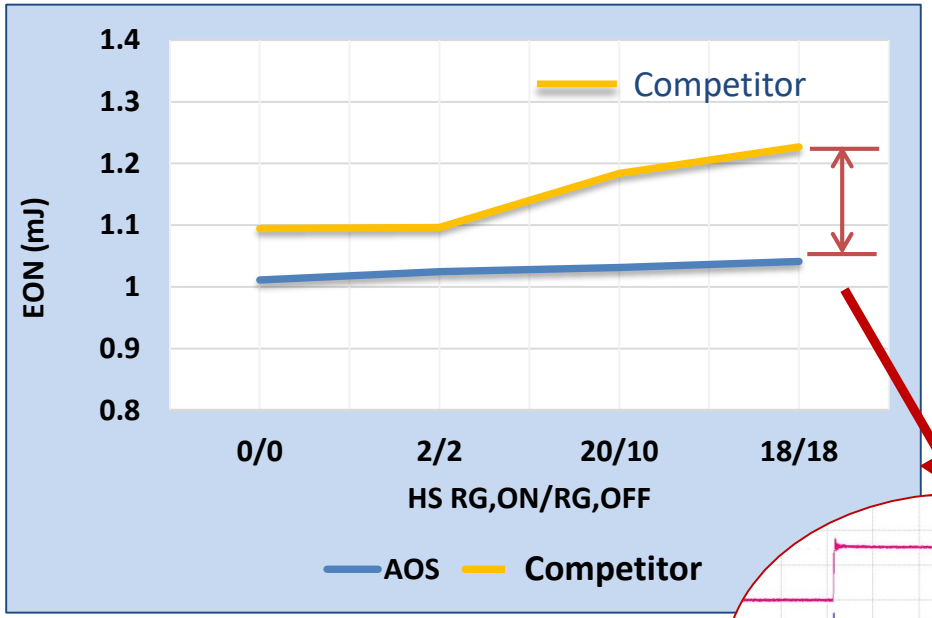
1200V SiC MOSFETs: Shoot-Through Testing

Switching reduces effective Vth at high dV/dt

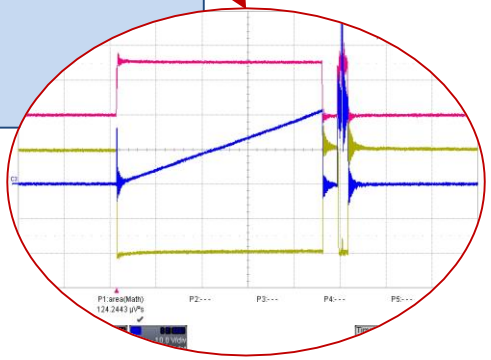


➡ Measure E_{ON} of LS device with HS variable $R_{G,OFF}$

- V_{DC}=800V, I_D=40A, upper switch Vgs=0V
- *dV/dt ~ 80V/ns*



> 20% E_{ON} increase



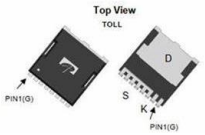
650V MOSFETs / Double Pulse Shoot-Through Test

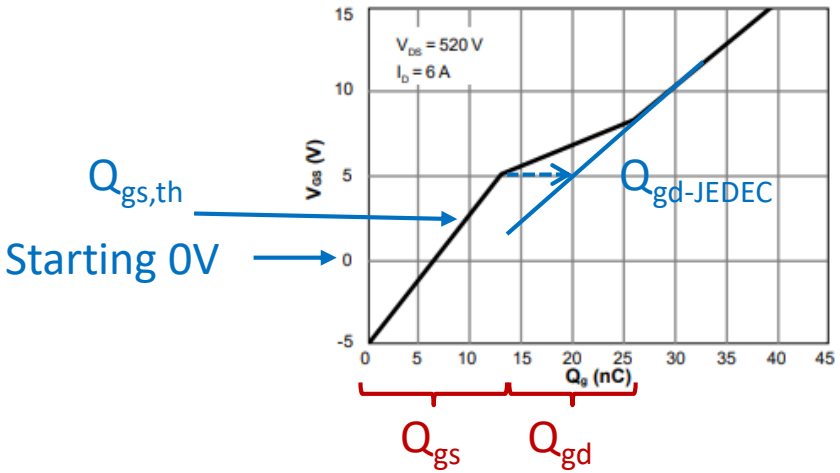
- **650V Datasheet Important Parameters**

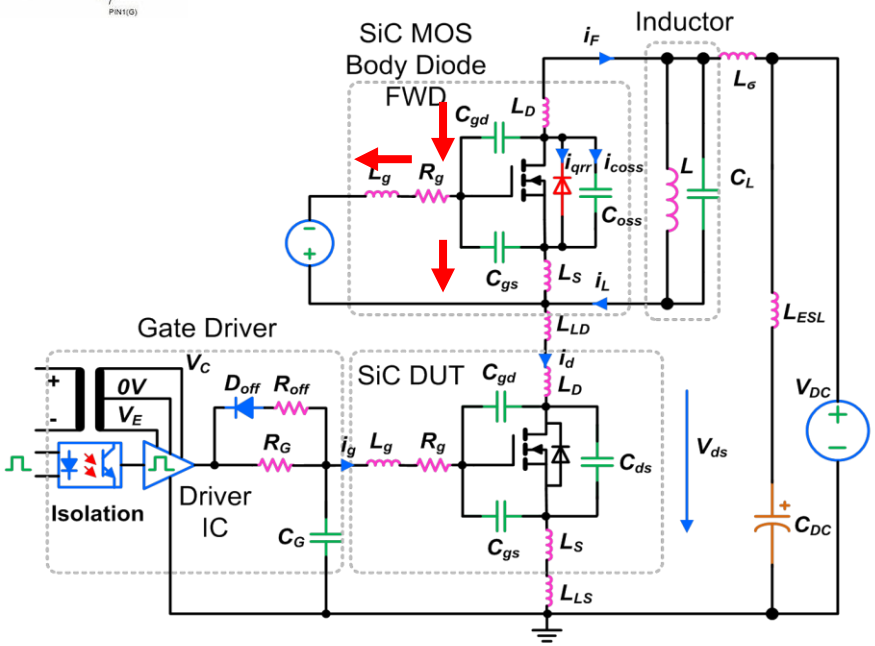
  → **Qg: Not all measured the same**

SiC MOSFET	V_{TH} (V)	Q_{gs} (nC)	$Q_{gs,th}$ (nC)	Q_{gd} (nC)	$Q_{gd\text{-}JEDEC}$ (nC)	$R_{G,INT}$ (Ω)	FOM
AOS Planar	2.8	5	1.7	12.9	8	2.2	.56
Trench	4.5	5	3	12.5	3.5	5.1	.76
Trench	4.5	11	10	19	10	12	.38
Planar	2.3	7	2	17	12.5	3	.12
Planar	2.9	10	4.5	16	14	5	.19

$$\text{Rough FOM} = \frac{V_{TH} \times \frac{Qgd}{Qgs}}{R_{G,INT}}$$



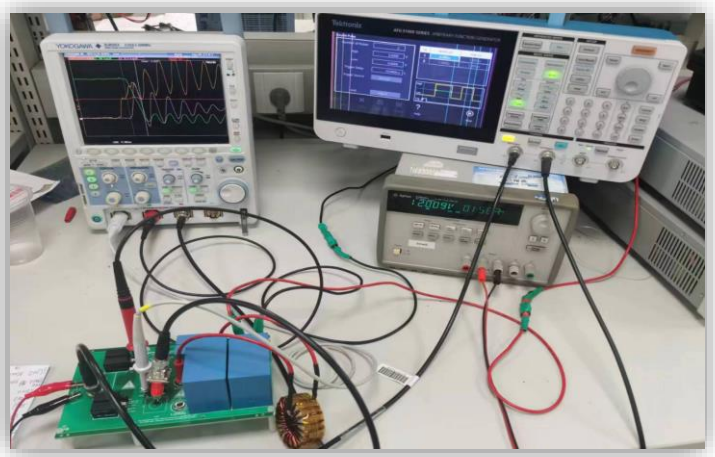


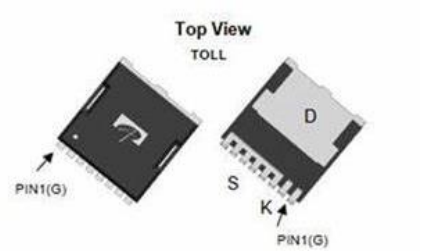


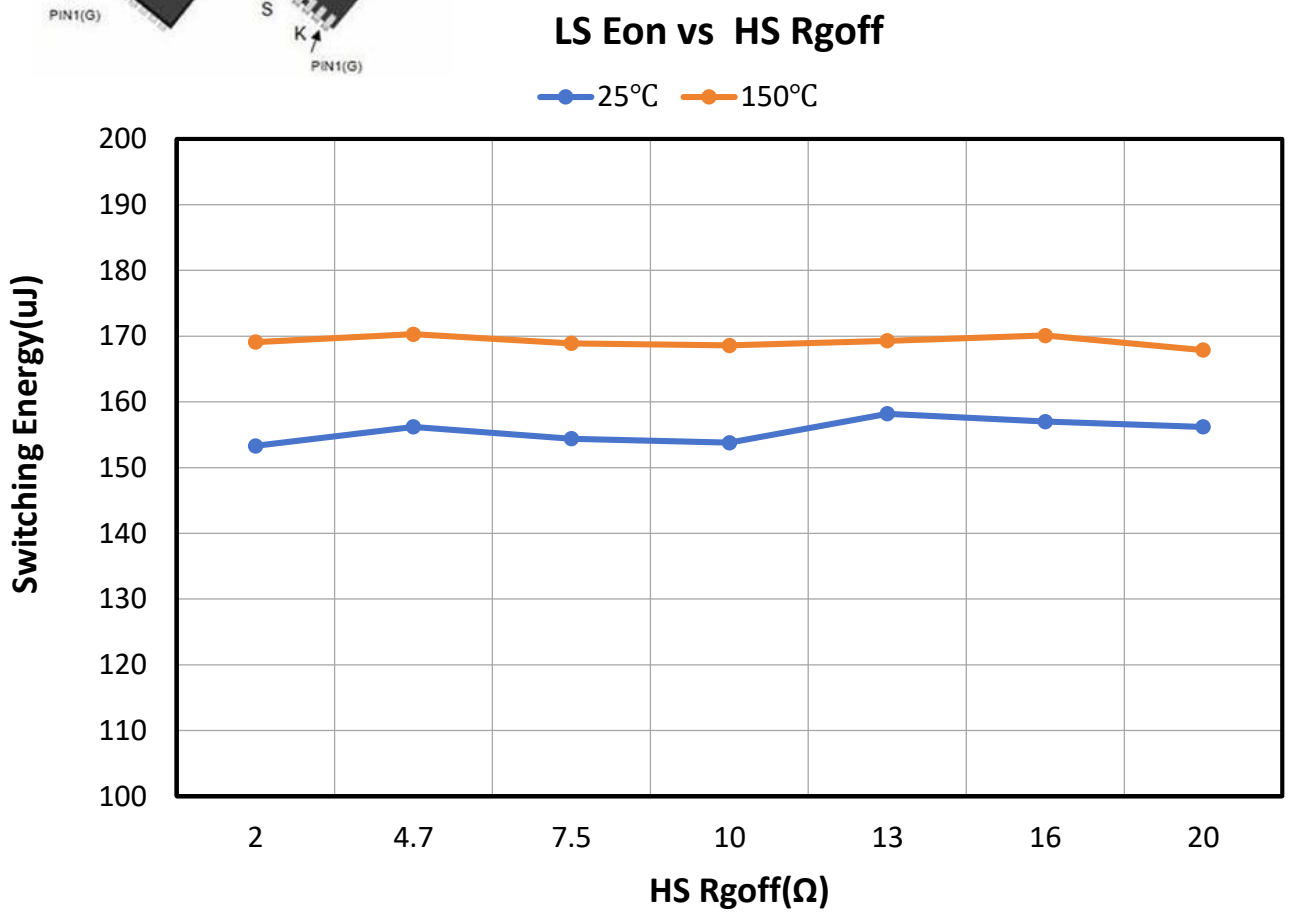
650V Double Pulse Shoot-Through Test

- **Test AOS Device Under Worst Case Device Conditions**

Test Conditions		
Bus voltage V_{DC}	400V	500V
Junction Temp. T_j	25℃	150℃
Switching dv/dt	42V/ns	84.4V/ns
HS Gate Off Resistance $R_{goff(HS)}$	2~20Ω	2~20Ω
LS Gate On Resistance $R_{gon(LS)}$	2Ω	2Ω
Drain-Source Current I_D	40A	40A
HS&LS Gate Voltage	0/+18V	0/+18V



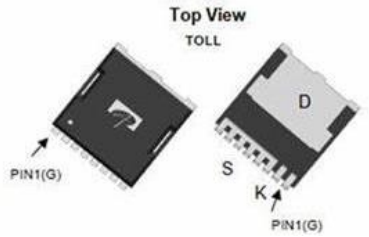




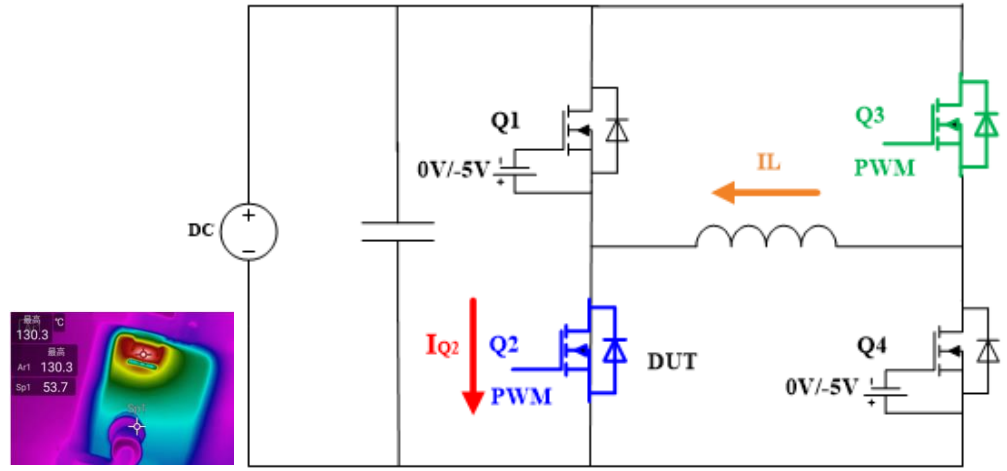
650V SiC Cross-Conduction Burn-in Test

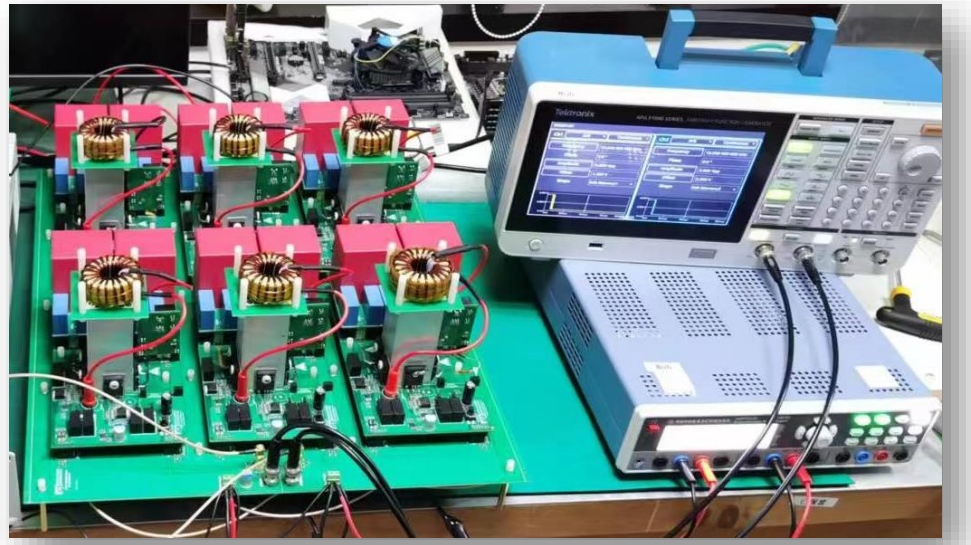
- **Test Set-up and Topology**
  - **Burn-in test is used to simulate the real working condition of SiC MOSFET with 0V turn-off voltage in application.**

Conditions	
Bus voltage V_{DC}	500V
Peak Current I_{DM}	50A
System Switching Frequency F_S	10kHz
HS&LS Gate Voltage	0/+18V
HS Gate Off Resistance $R_{goff(HS)}$	20Ω
LS Gate On Resistance $R_{gon(LS)}$	2Ω
Junction Temp. T_j	150℃



Burn-in Topology

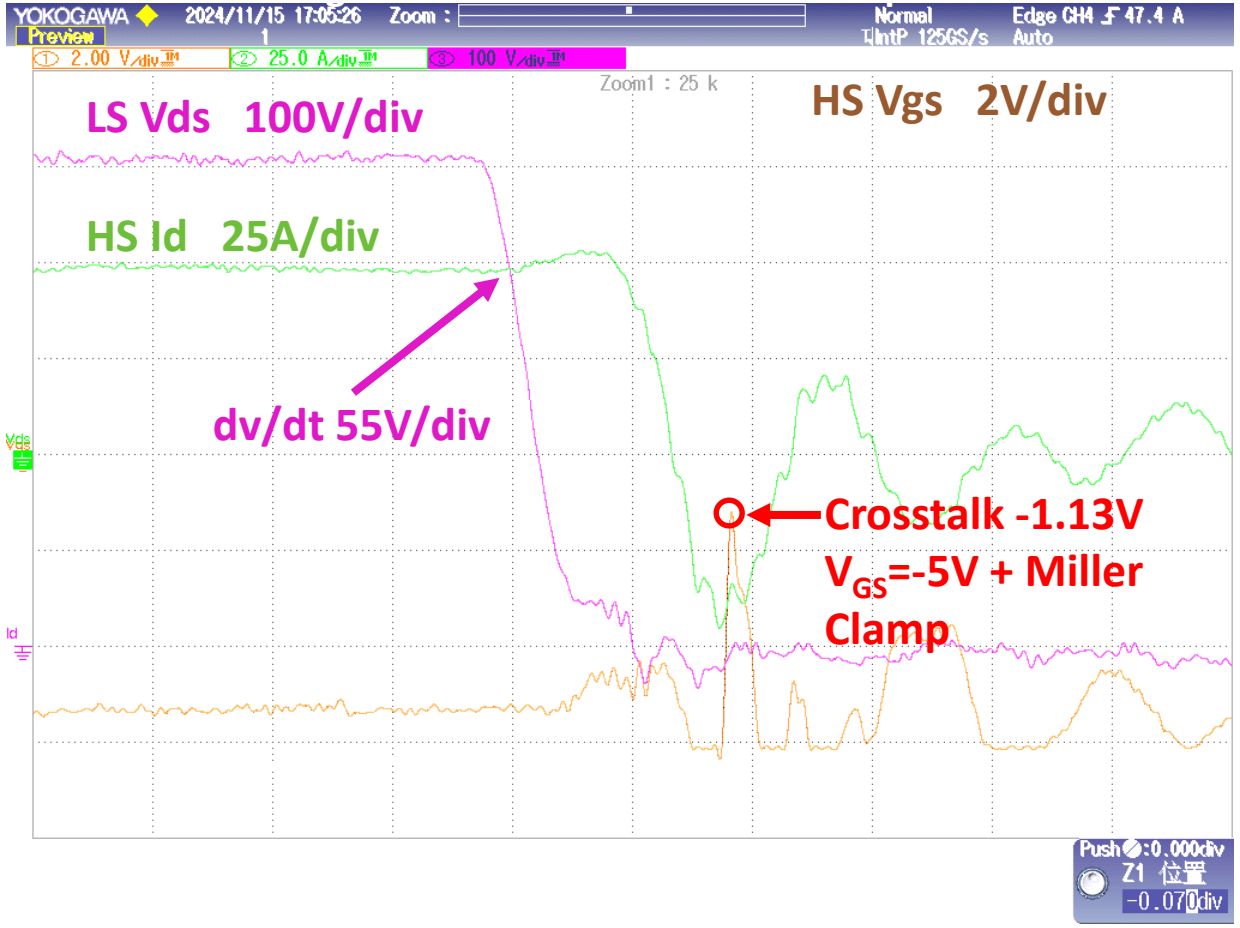




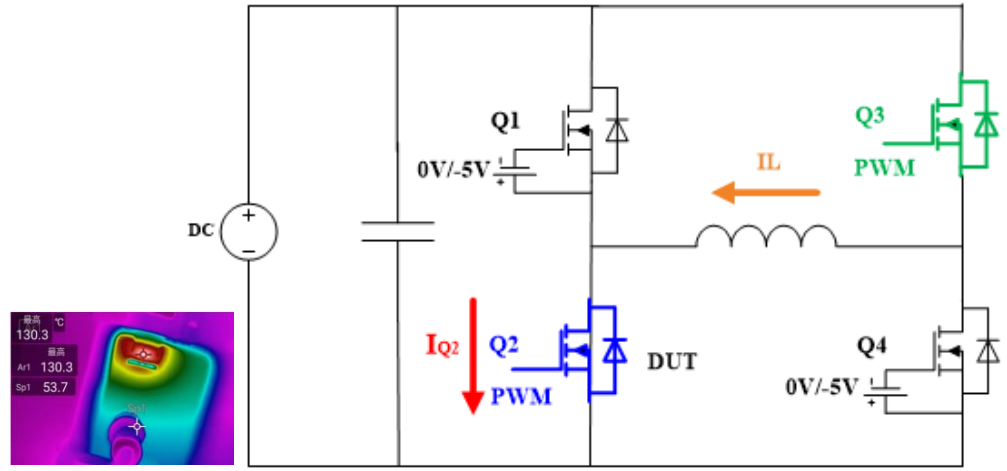
650V SiC Cross-Conduction Burn-in Test

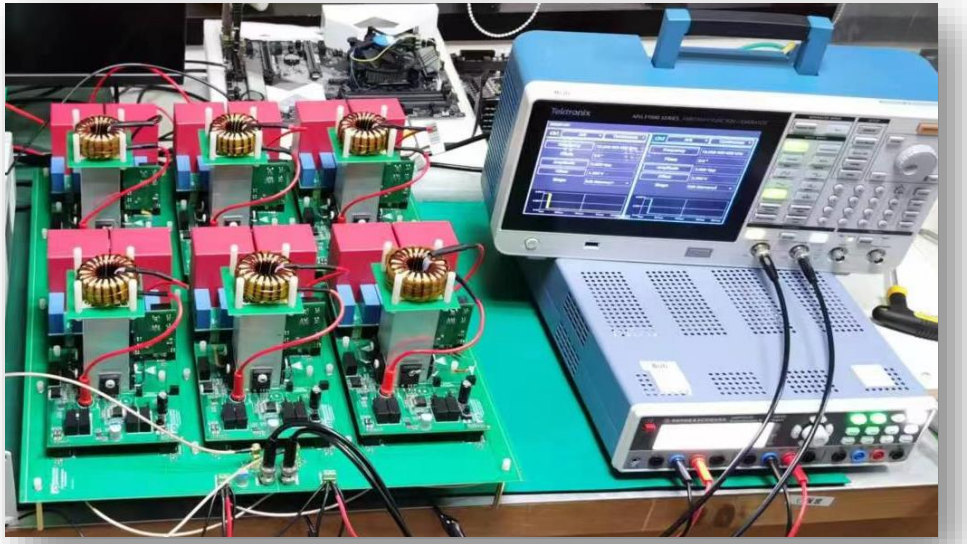
- **Benchmark test:**
  - V_{DS}=500V, T_j=150C, dV/dt=55V/ns
  - V_{GS}=-5V + Miller Clamp → Baseline Current

HS Vgs and Current Waveforms Comparison



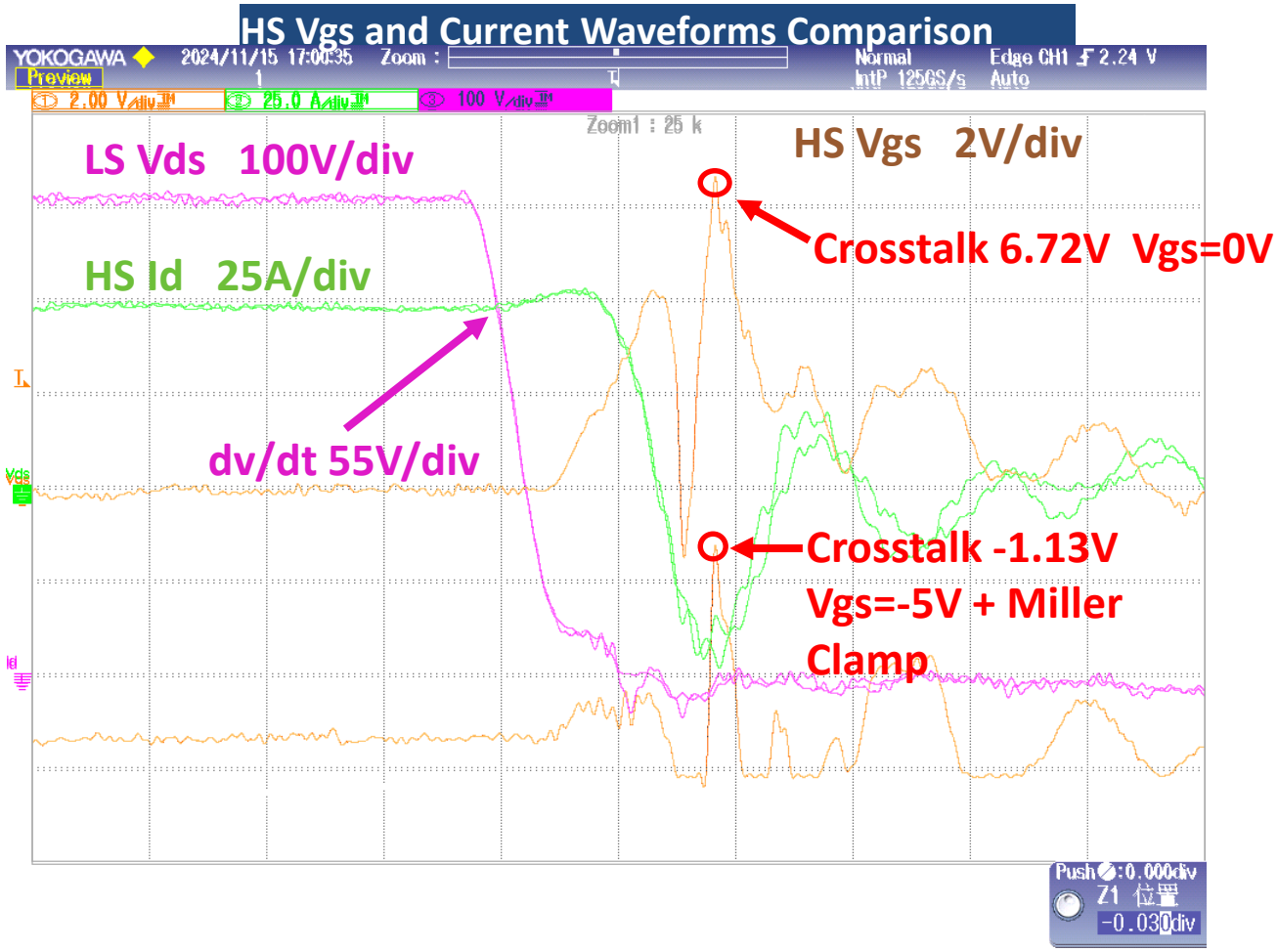
Burn-in Topology



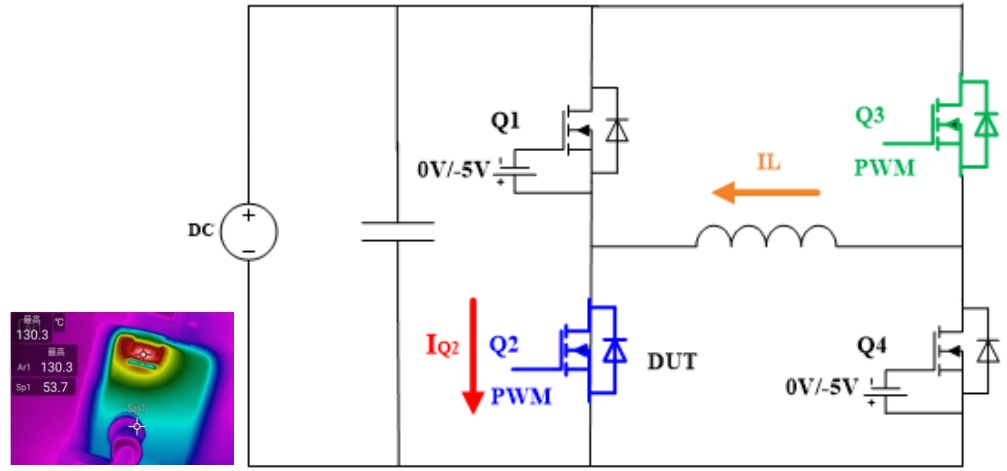


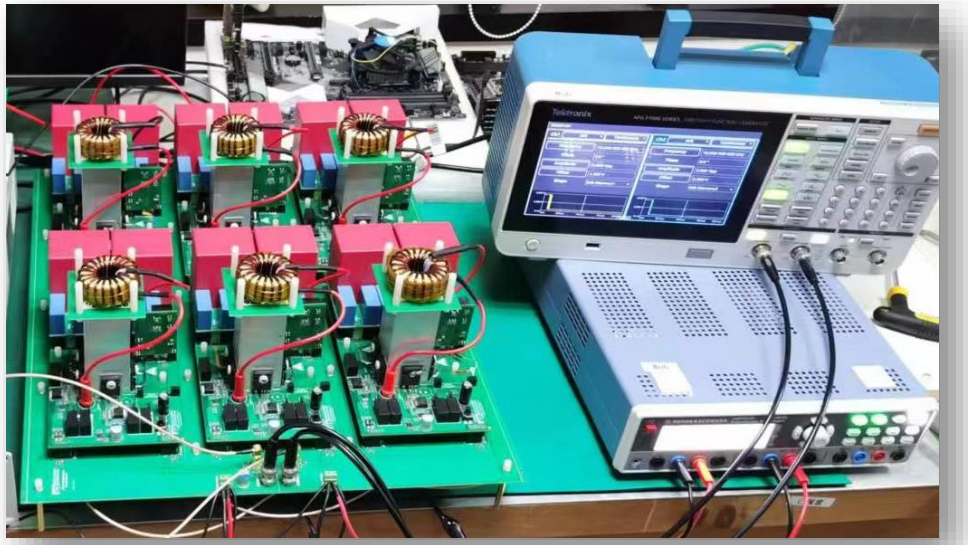
650V SiC Cross-Conduction Burn-in Test

- **Benchmark test:**
  - V_{DS}=500V, T_j=150C, dV/dt=55V/ns
  - V_{GS}=0V → No Change in Current! = No shoot-through!



Burn-in Topology





Summary

Question: Can I switch a SiC MOSFET at $V_{GS,off}$=0V drive conditions?

Answer: Yes!

- → Use optimized SiC MOSFET with low $R_{G,INT}$, Good Q_{gs}/Q_{gd}, higher V_{TH}, Low DIBL
- → Optimized Layout
- → Manage dV/dt
- → Gate Driver with Miller Clamp
- → Evaluate over worst case conditions

Thank You!