Riding the Second Wave of SiC: Power Packaging

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Bodo's Wide Bandgap Event 2024

Making WBG Designs Happen

SiC

Riding the Second Wave of Silicon Carbide (SiC)

First Wave

SiC die in existing packages

Second Wave

SiC die in higher performing packages

Third Wave

Higher Voltage SiC Solutions

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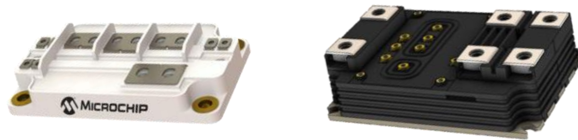
Package Importance, Trends and Challenges

- **While SiC technology is advancing rapidly, the packaging technology seemed to be relying on the past convention**
- **Current packaging development pointing to technical challenges**
  - Electrical domain: electrical parasitics of the package, gate driver consideration (drain kelvin link)
  - Thermal domain: low SiC die size requires high thermal performance
  - Materials and interconnection: high temperature operations is limited
  - Mechanical domain: pinout design for paralleling, intelligent DC links connection, gate drivers' consideration
  - Problem of second source: slow down adaptation of a new advanced package

Toward high power, symmetrical and low inductance layouts



Toward easy assembly, pinout and layout optimization for various topologies

Toward high semiconductor content integration

TO247-4

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TO-247 Performance Improvement

Source sense pin for faster turn on and lower switching losses

1200V, 80 mΩ mSiC™ MOSFET

R_G = 5Ω, V_{DS} = 750V, V_{GS} = -5V/20V, T_A = 25°C

E_{total} [mJ]

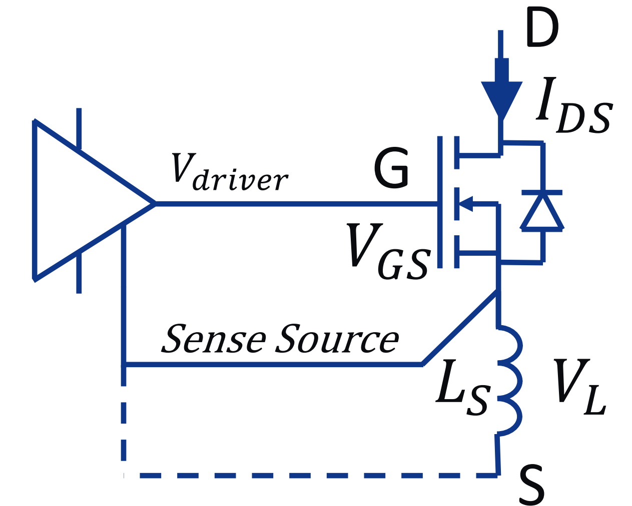
2,5
2,0
1,5
1,0
0,5
0,0

10 20 30 40 50

I_{DS} [A]

TO-247-3
TO-247-4

-69%



$$V_{GS} = V_{driver} - L_s \frac{dI_{DS}}{dt}$$

$$V_{GS} = V_{driver} - V_L$$

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Pushing Beyond The TO-247

Source sense pins and top-side cooled

1200V, 180 mΩ mSiC™ MOSFET

R_G = 5Ω, V_{DS} = 800V, V_{GS} = -5V/20V, T_A = 25°C

180 mΩ, 1200V
TO247-3 Package
(MSC180SMA120B)

180 mΩ, 1200V
D2PAK Package
(MSC180SMA120SA)

180 mΩ, 1200V
PSMT Package
(MSC180SMA120SC)

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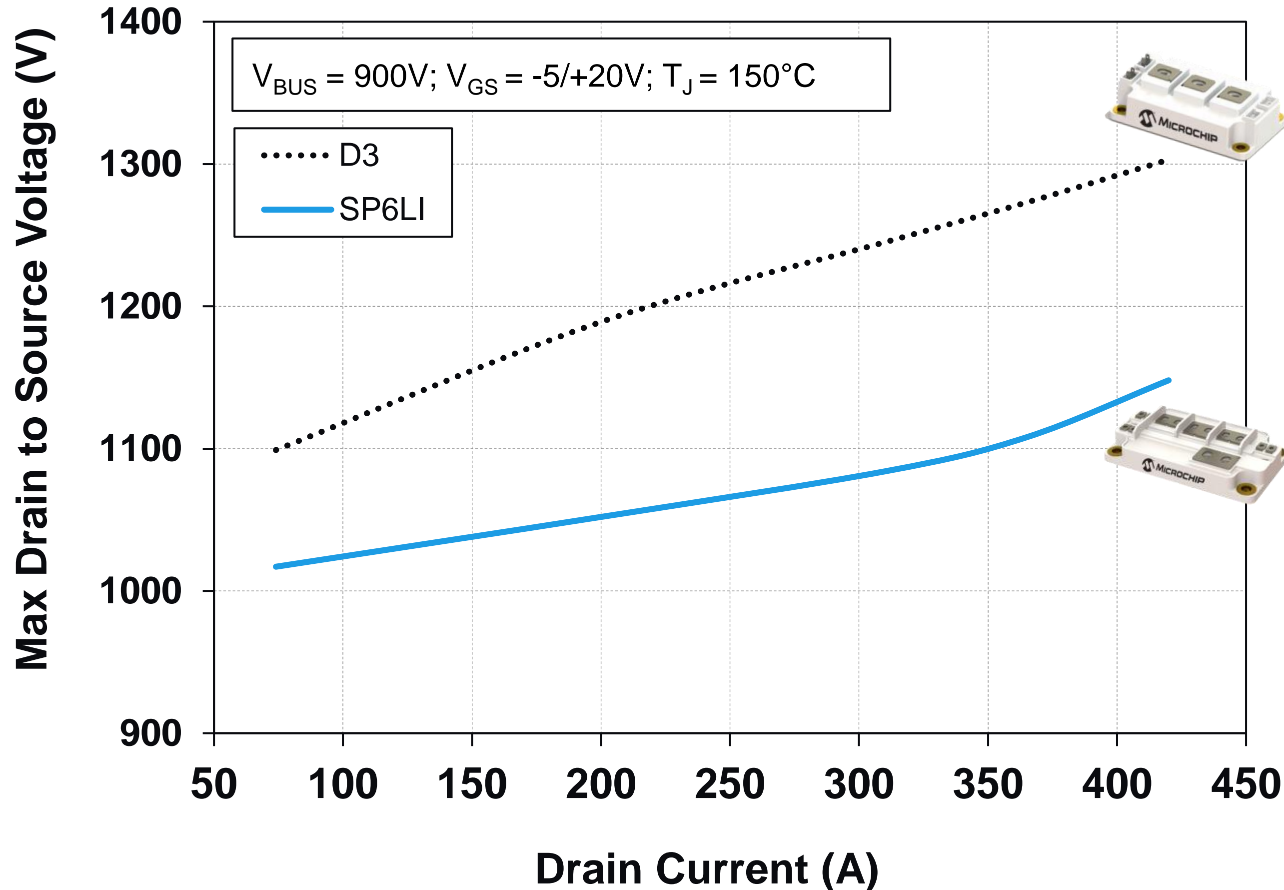
Extremely Low Stray Inductance

Benefit 1 – Reduced voltage overshoot



Designers can use lower rated devices and still have margin against overshoot

- Lower device cost
- Greater system efficiency

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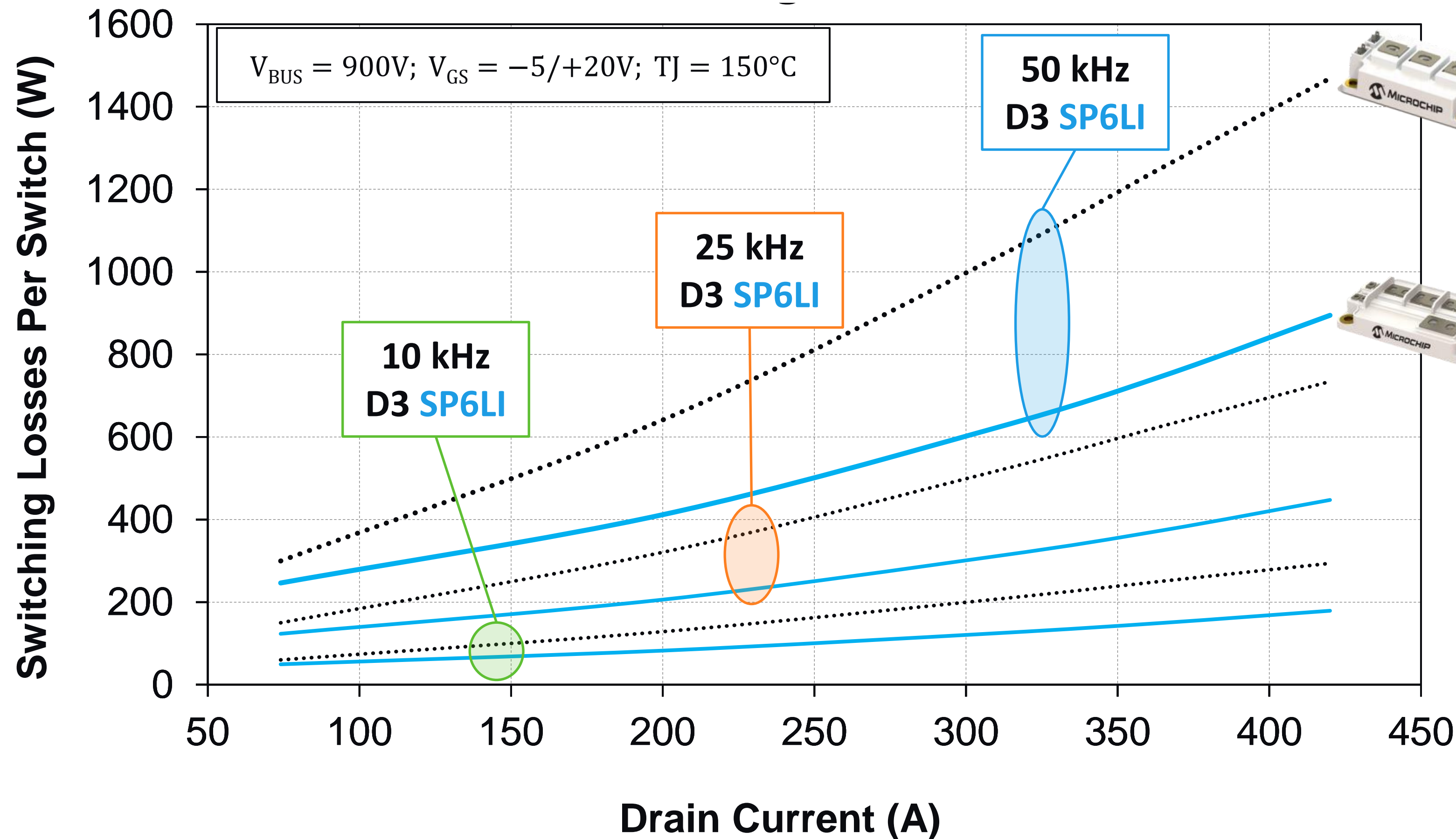
Extremely Low Stray Inductance

Benefit 2 – Greater efficiency across wide working conditions



Total switching losses are 20-40% lower

Effects are more pronounced at higher switching frequency and drain current

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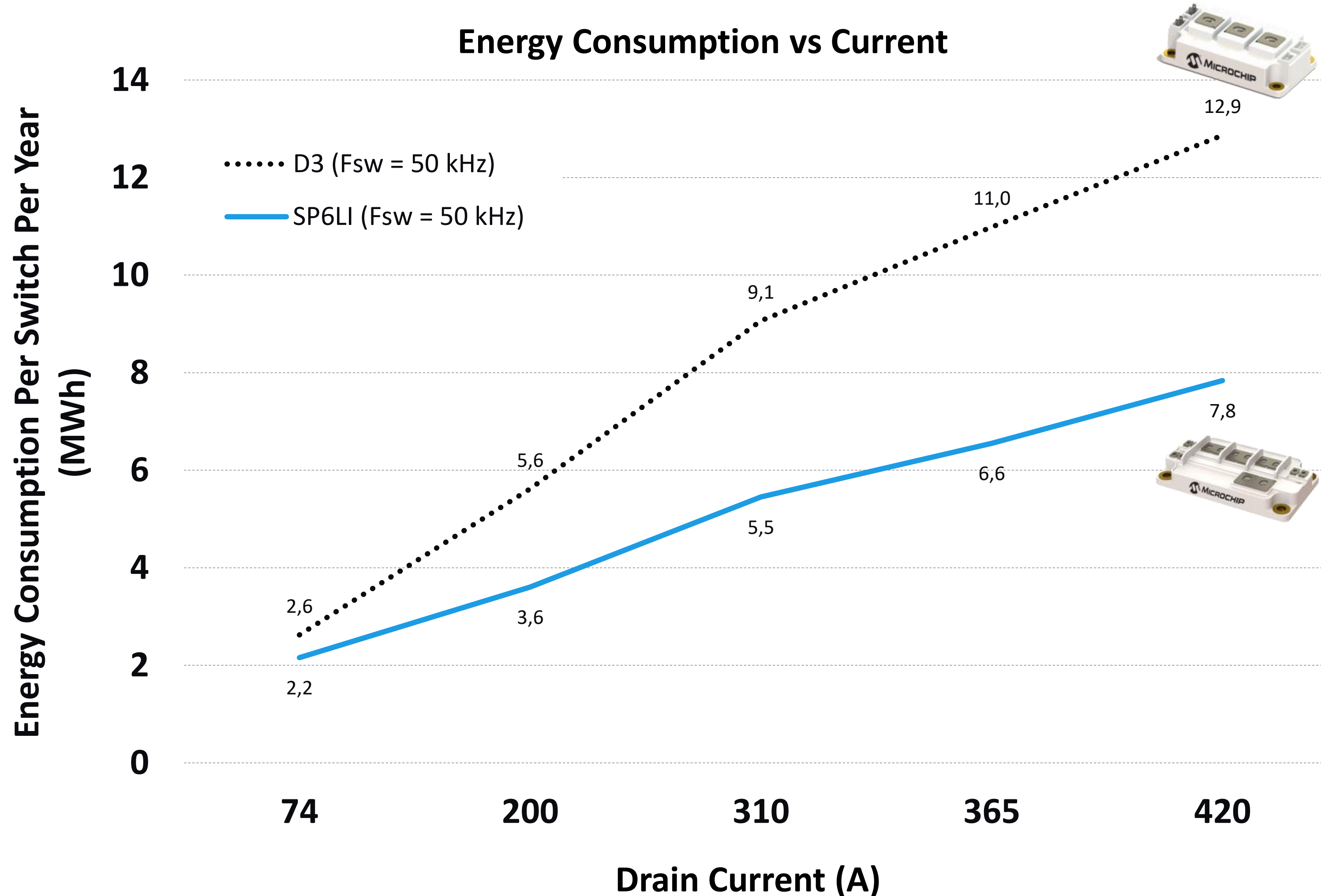
Extremely Low Stray Inductance

Benefit 3 – Reduced cost of ownership



	10 kHz	25 kHz	50 kHz
D3	2.6	6.4	12.9
SP6LI	1.6	3.9	7.8

Total switching losses per switch per year at 420A, in units of MWhs

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Summary

Broad market acceptance that SiC saves cost at the system level

To get even more out of SiC, new packaging is required to make systems more efficient, compact, and longer-lasting

Today we have looked at the impact of parasitic inductance

Comparing the SP6LI to the common 62 mm package, the end user can save over $1,000 per module per year

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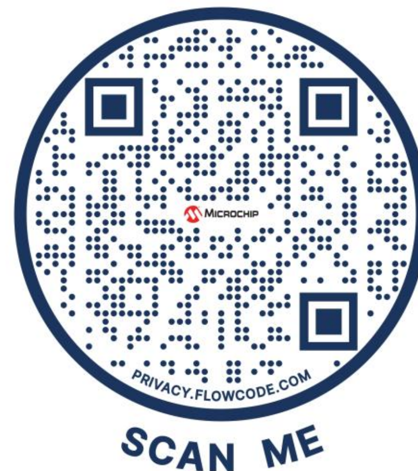

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