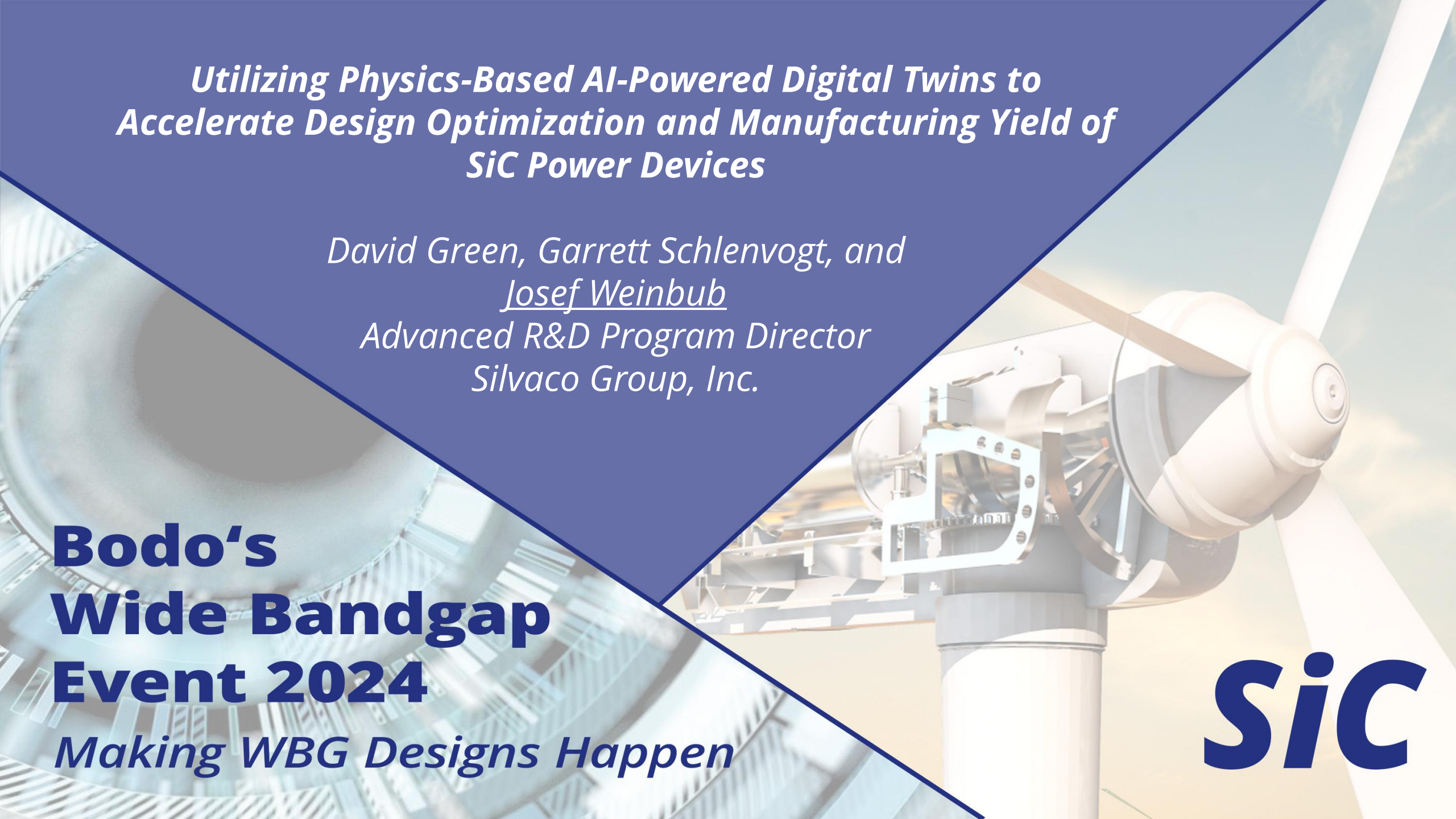
Utilizing Physics-Based AI-Powered Digital Twins to Accelerate Design Optimization and Manufacturing Yield of SiC Power Devices

David Green, Garrett Schlenvogt, and Josef Weinbub
Advanced R&D Program Director
Silvaco Group, Inc.



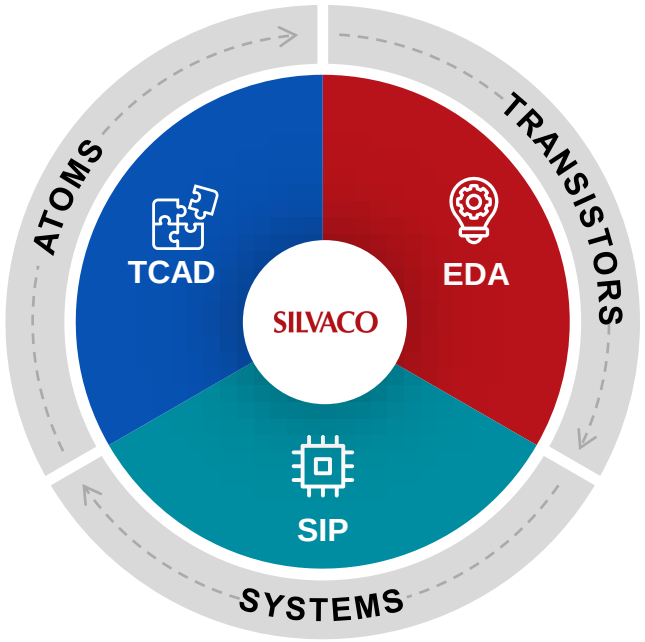
Bodo's Wide Bandgap Event 2024

Making WBG Designs Happen

SiC

Silvaco at a Glance

Enhancing Design Productivity and Production Efficiency through Software Innovation and Automation



Automotive | IoT | 5G / 6G | Display | Memory | HPC | Power

Silvaco Leadership

600+ Customers

#2[(1)] Global TCAD revenue

200+ University Customers

260+ Employees

- **TCAD Adoption 4 of 10** — Largest SiC, GaN Power Device Providers[3]
- **EDA Adoption 7 of 10** — Largest flat panel display companies[1]
- **EDA Adoption 6 of 10** — Largest semiconductor companies[2]
- **TCAD Adoption 8 of 10** — Largest flat panel display companies[1]

Global Presence

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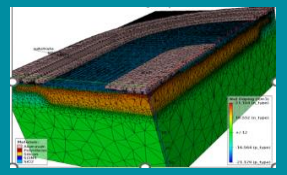
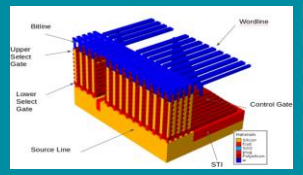
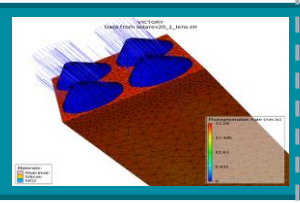
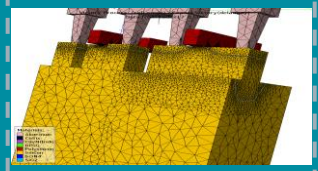
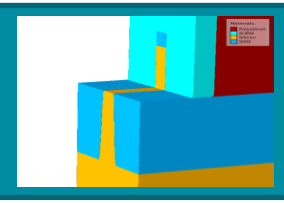
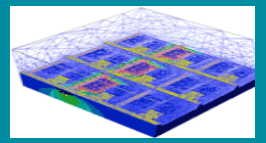
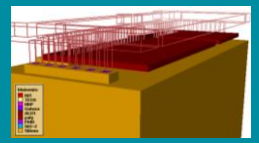
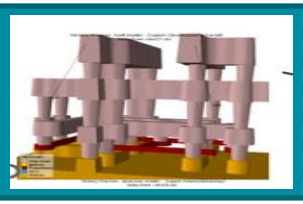
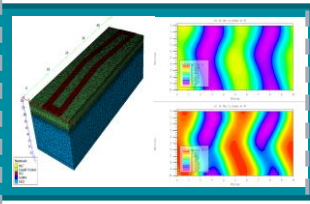
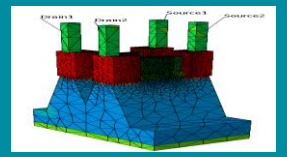
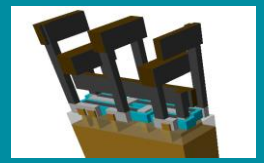
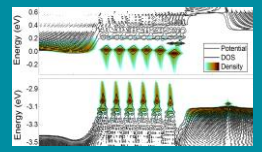
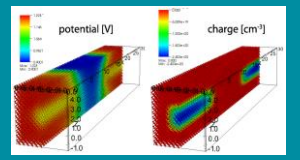
Silvaco TCAD

Enabling Semiconductor and Photonics Technology Innovation

	Display	Power	Memory	Photonics	CMOS	Adv. CMOS
Victory TCAD 2D/3D process and device simulation						
Victory RCX Pro In-house 3D field solver + RC extraction						
Victory Atomistic Purdue-based quantum transport solver						

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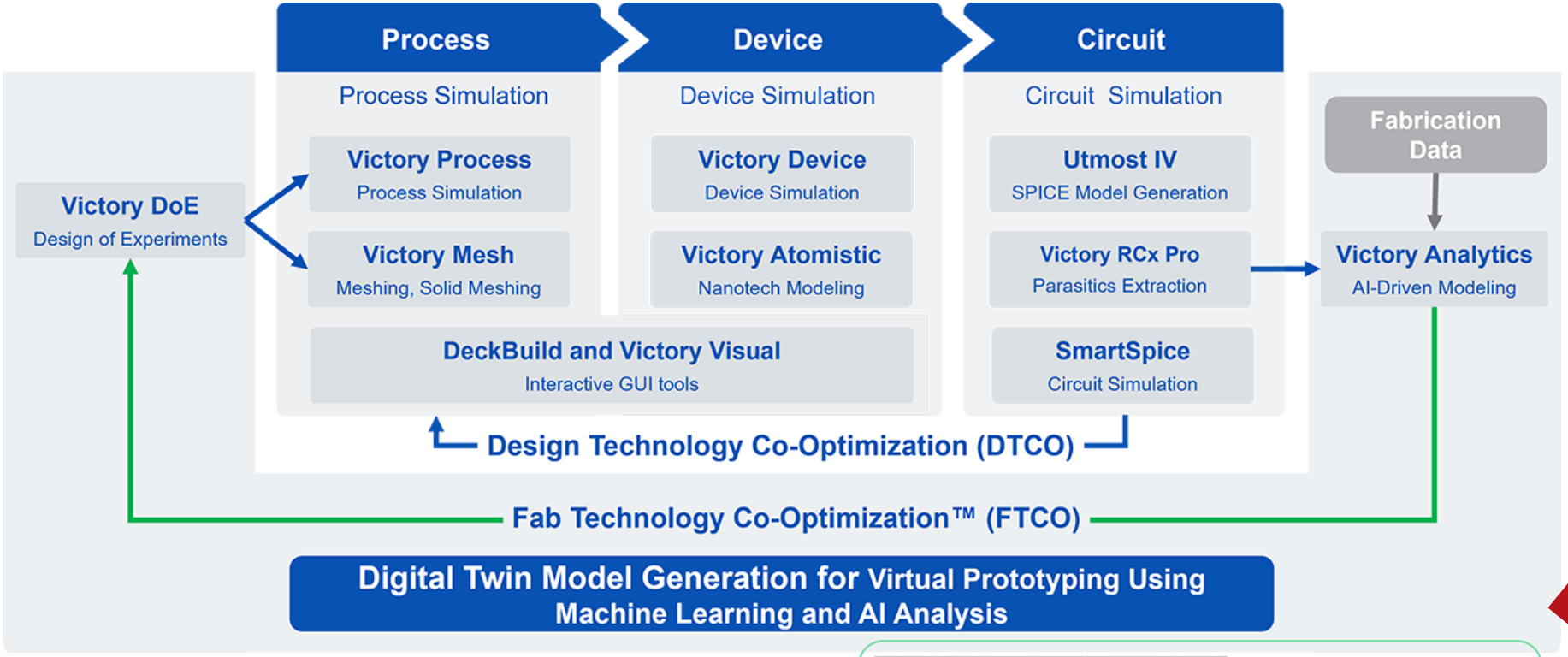
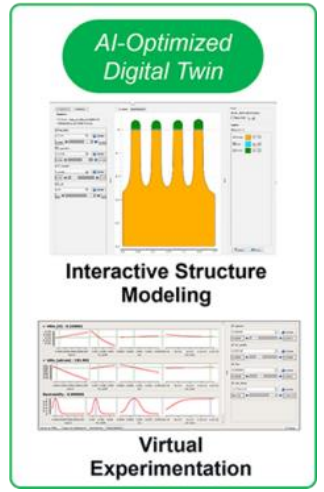
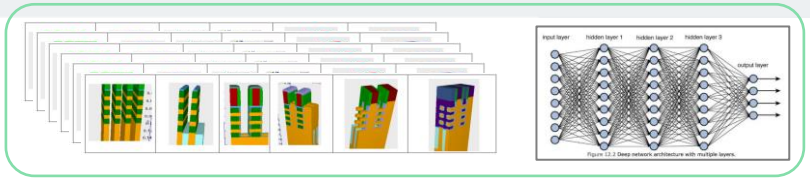
Fab Technology Co-Optimization (FTCO™) from Silvaco

Removing Cost of Trial-and-Error Using AI-Driven Models Through Digital Twins







TCAD/Simulation Engineer

Fab/Product/Process Engineer

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FTCO™ – Executive Summary

AI Modeling on Amalgamated Fab and Digital Twin Data

- Enables optimization of manufacturing processes, reduced costs, increased yields and ultimately leads to higher-quality semiconductor devices and improved manufacturing productivity.
- Leverages artificial intelligence (AI), machine learning (ML) and physical simulation in concert with experimental data to generate a **Digital Twin**, mirroring the form, fit and function of the physical world.
- A Digital Twin
  - allows for interactive structure modeling, virtual experimentation and shortens learning cycles
  - is user-friendly and accessible to engineers not traditionally using physics-based simulation
  - provides a single source of data where all specialists can understand the effects of development changes:
    - Integrated full (or partial) flow from Process, Device, even to Parasitic Extraction and SPICE
    - Changes upstream/downstream - cause / effect
    - Breaks down data ownership silos
    - To provide design targets and receive input specification

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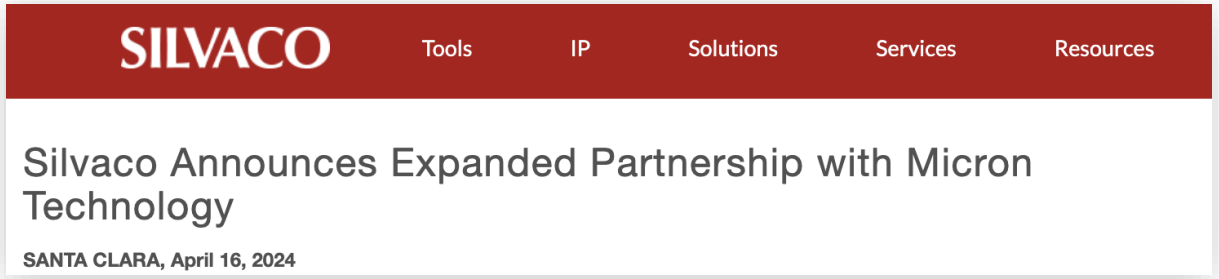
FTCO™ – Optimizing Memory Devices

In Partnership with Micron Technology, Inc.

- Goal
  - Use production data and physics-based simulation in concert:
    Focus on etching, deposition, and mechanical stress
  - Leverage AI/ML to analyze data, understand what experiments (real, virtual) are needed next
  - Enable fabrication, process, and product engineers to have a user-friendly Digital Twin, interactive in real time

- Outcome
  - Accelerate design and pathfinding for memory product development



> *"Micron is excited to strengthen our partnership with Silvaco. Silvaco's AI and digital twin solution is enabling us to accelerate our groundbreaking advancements in memory and storage."*

Dr. Gurtej Sandhu
Principal fellow of Technology Pathfinding
IEEE Life Fellow
Micron Technology, Inc.

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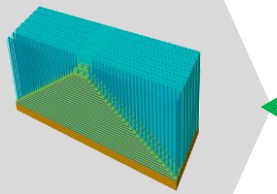
Digital Twin – A Physics Based Digital Counterpart

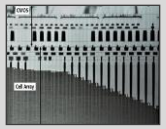
Expanding FTCO™ to other Silvaco Supported End-Applications

Digital Twin ⟷ **Real World**

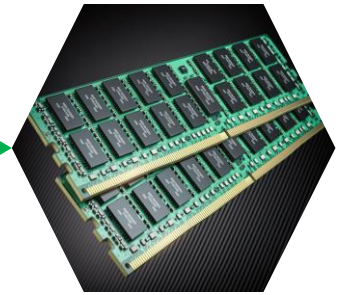


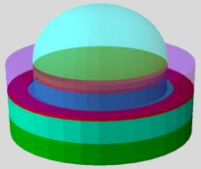
Memory Array

Electron Microscope View



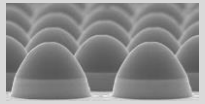
Wafer





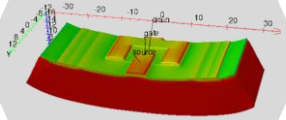
MicroLED

Electron Microscope View



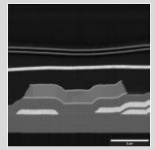
Display Panel

Digital Twin ⟷ **Real World**

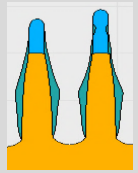


Flexible Display

Electron Microscope View



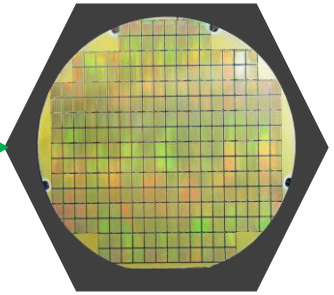
OLED



FinFET Transistor

Electron Microscope View

Wafer



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FTCO™ – Optimizing Power Semiconductor Devices

AI Modeling on Amalgamated Fab and Digital Twin Data

Consider Wide Bandgap (SiC / GaN):

- Materials/processes are more complex than Si
- Process is still maturing, reining in adoption rate
  - *"Every OEM offering a SiC MOSFET is debugging it on the side"* [1]
- What are the big challenges to solve?
  - Gate Oxide Quality – traps / faults / variation
  - Mobility Modelling – many components, many parameters
  - Substrates / Epitaxy - quality / traps
  - Aging - humidity, reliability
  - Mechanical stress / strain
  - Design-aware technology development – not just targeting DC behavior but considering transient switching performance as part of the R&D and manufacturing ramp process
- Developing digital twin models can help to address these challenges

[1] https://www.eetimes.eu/the-challenges-for-sic-power-devices/

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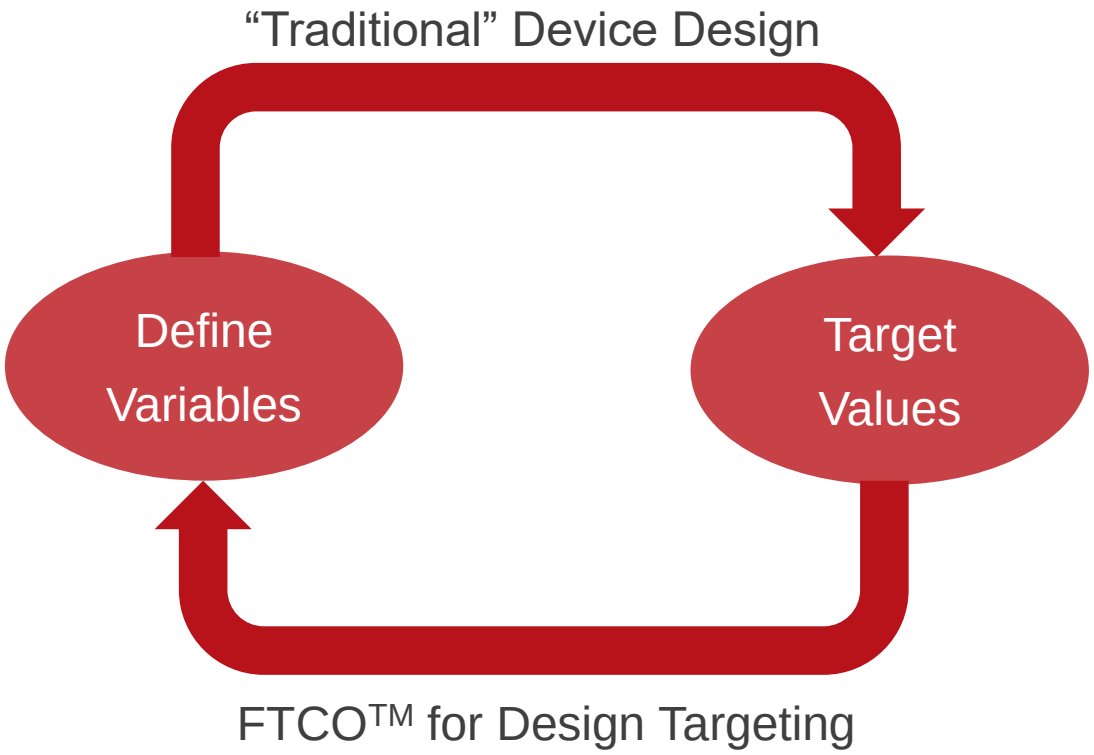
Using FTCO™ for Design Targeting

Reversing Traditional Device Design Process

- Design Targeting:
  - Provide design targets, define design inputs
  - Digital twin model returns input values to achieve the targets
- Enables more efficient and more precise specification
- Determines dominant inputs to rapidly understand and optimize technology
- What does the engineer need to care about?



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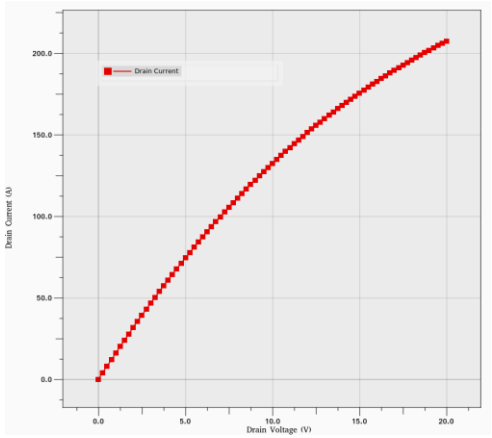
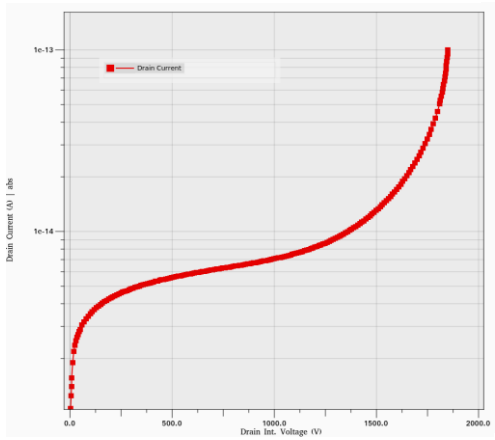
Case Study: 1200 V SiC DMOS Design Targeting

Process Simulation and Device Characterization

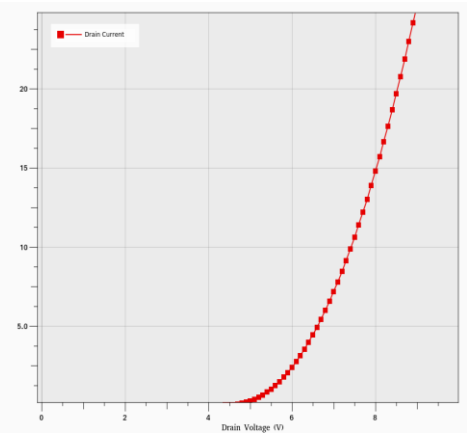
- Design Targets:
  - BV=1800 V (derated to 1200 V), Vth=3 V, lowest RdsOn possible
- Design Inputs:
  - Doping: NDrift, JFET implants (x4 dose/energy), PWell implants (x4 dose/energy)



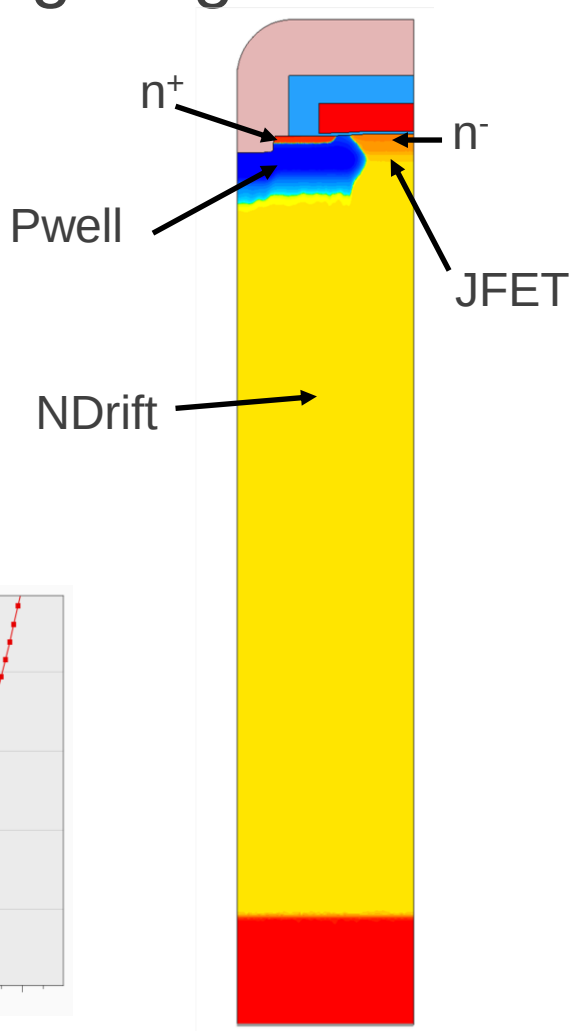
On-state



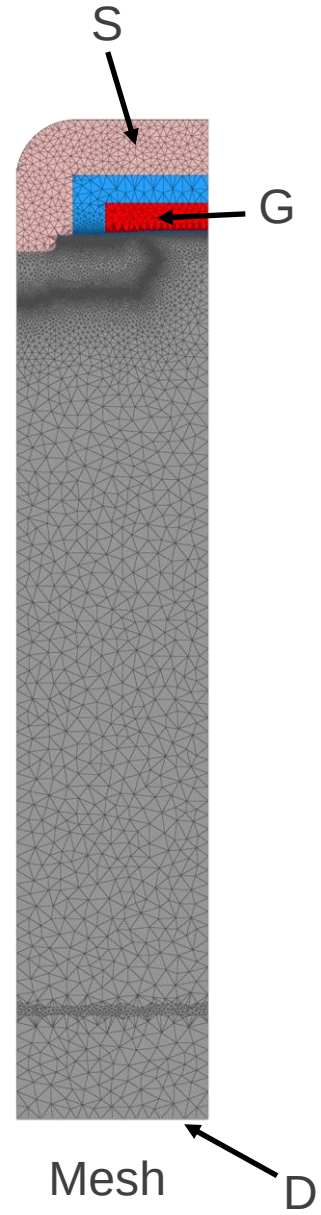
Breakdown



Threshold



Net Doping



Mesh

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Screening Inputs

Intelligent / Optimum Design of Experiments (DoE)

Find the dominant input factors that are affecting the outputs

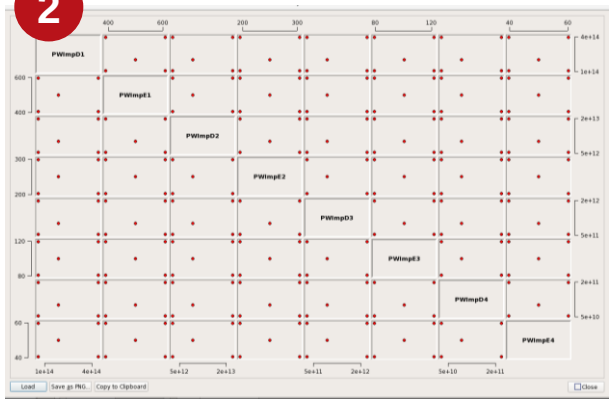
1. Define range on chosen variables
2. “Smart DoE” methodology (D-optimal design) - efficient exploration of effects variables have on design
3. Run the DoE on the Digital Twin and Collect Data

1

	Init	Low	High
PWImpD1	2.000e+14	1e+14	4e+14
PWImpE1	500	400	600
PWImpD2	1.000e+13	5e+12	2e+13
PWImpE2	250	200	300
PWImpD3	1.000e+12	5e+11	2e+12
PWImpE3	100	80	120

FF OFAT

2



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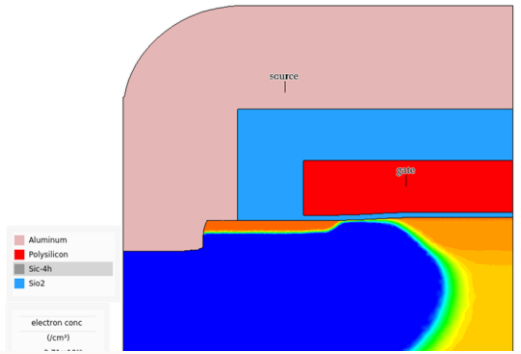

Row	Module	Variable	1	2	3	4	5	6	7	8	9	10	11
8	Channel_Spacer		n113	n114	n115	n116	n117	n118	n119	n120	n121	n122	n12
9	Source_Doping		n158	n159	n160	n161	n162	n163	n164	n165	n166	n167	n16
10	Activation_Anneal		n203	n204	n205	n206	n207	n208	n209	n210	n211	n212	n21
11	Gate_Oxidation		n248	n249	n250	n251	n252	n253	n254	n255	n256	n257	n25
12	Electrodes		n293	n294	n295	n296	n297	n298	n299	n300	n301	n302	n30
13	mesh		n338	n339	n340	n341	n342	n343	n344	n345	n346	n347	n34
14	Vt		n383	n384	n385	n386	n387	n388	n389	n390	n391	n392	n39
15	OnState		n428	n429	n430	n431	n432	n433	n434	n435	n436	n437	n43
16	BV		n473	n474	n475	n476	n477	n478	n479	n480	n481	n482	n48

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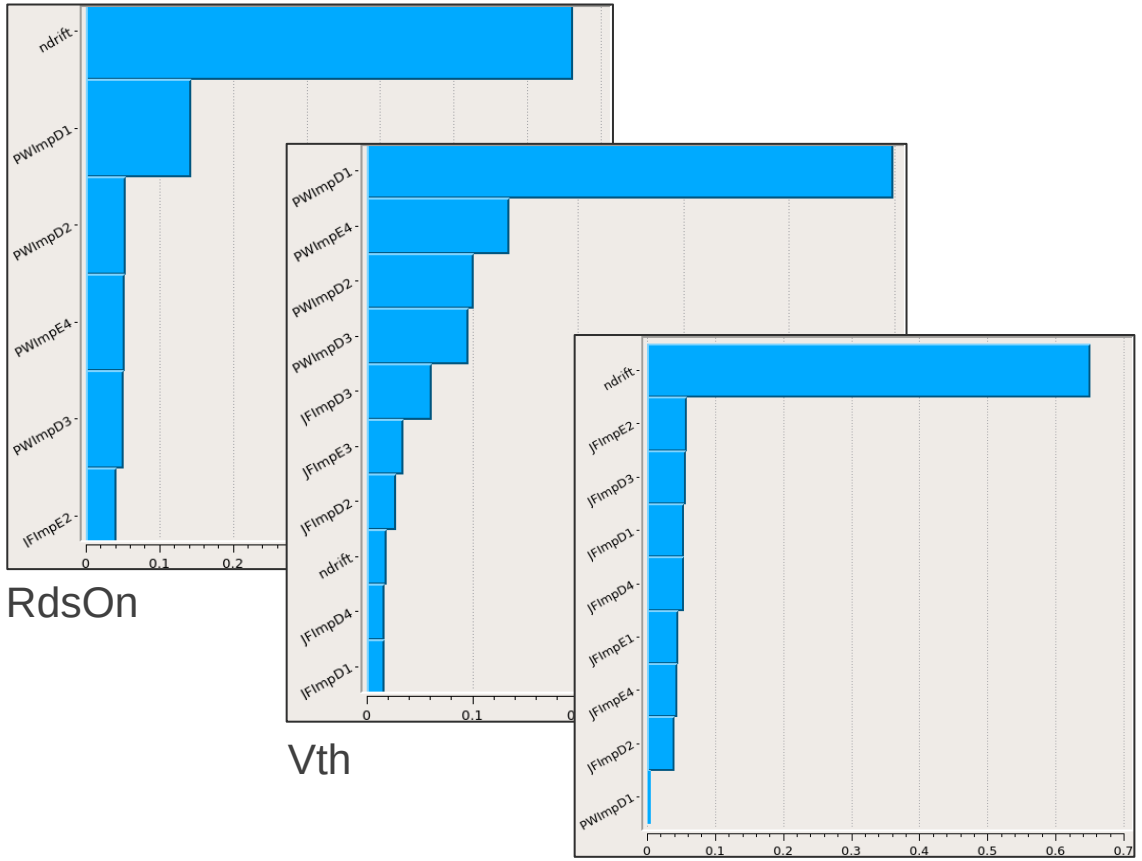
Identify Significant Variables Using ML

Use ML Neural Networks to Screen the Variables Using Smart-DoE Methodologies



Importance	Vth	RDSON	BV
1	**PWImpD1** ~0.5	**Ndrift** >0.6	**Ndrift** >0.6
2	**PWImpE4** >0.1	**PWImpD1** >0.1	JFImpE2 <0.1
3	**PWImpD2** ~0.1	**PWImpD2** <0.1	JFImpD3 <0.1
4	PWImpD3 <0.1	**PWImpE4** <0.1	JFImpD1 <0.1
5	JFImpD3 <0.1	PWImpD3 <0.1	JFImpD4 <0.1

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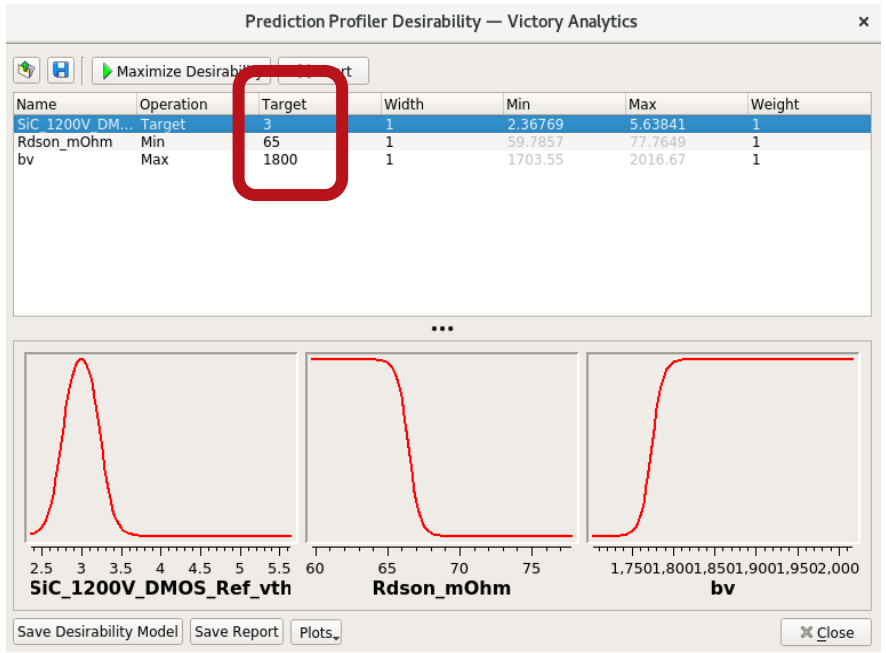
Optimization And Verification

Homing-in / Neural Network Regression

Optimization:

- Target 3 V for Vth
- Find minimum RdsOn
- 1800 V breakdown voltage



Neural Network Model

Input Values from NN Model

	Init
ndrift	9.32e15
PWImpD1	1.6e14
PWImpD2	5.26e12
PWImpE4	53

TCAD Verified Results

OUT:Vt	SiC_1200V_D...	2.98
OUT:OnState	Von	1.541
	Rdson_mOhm	61.64
OUT:BV	bv	1762

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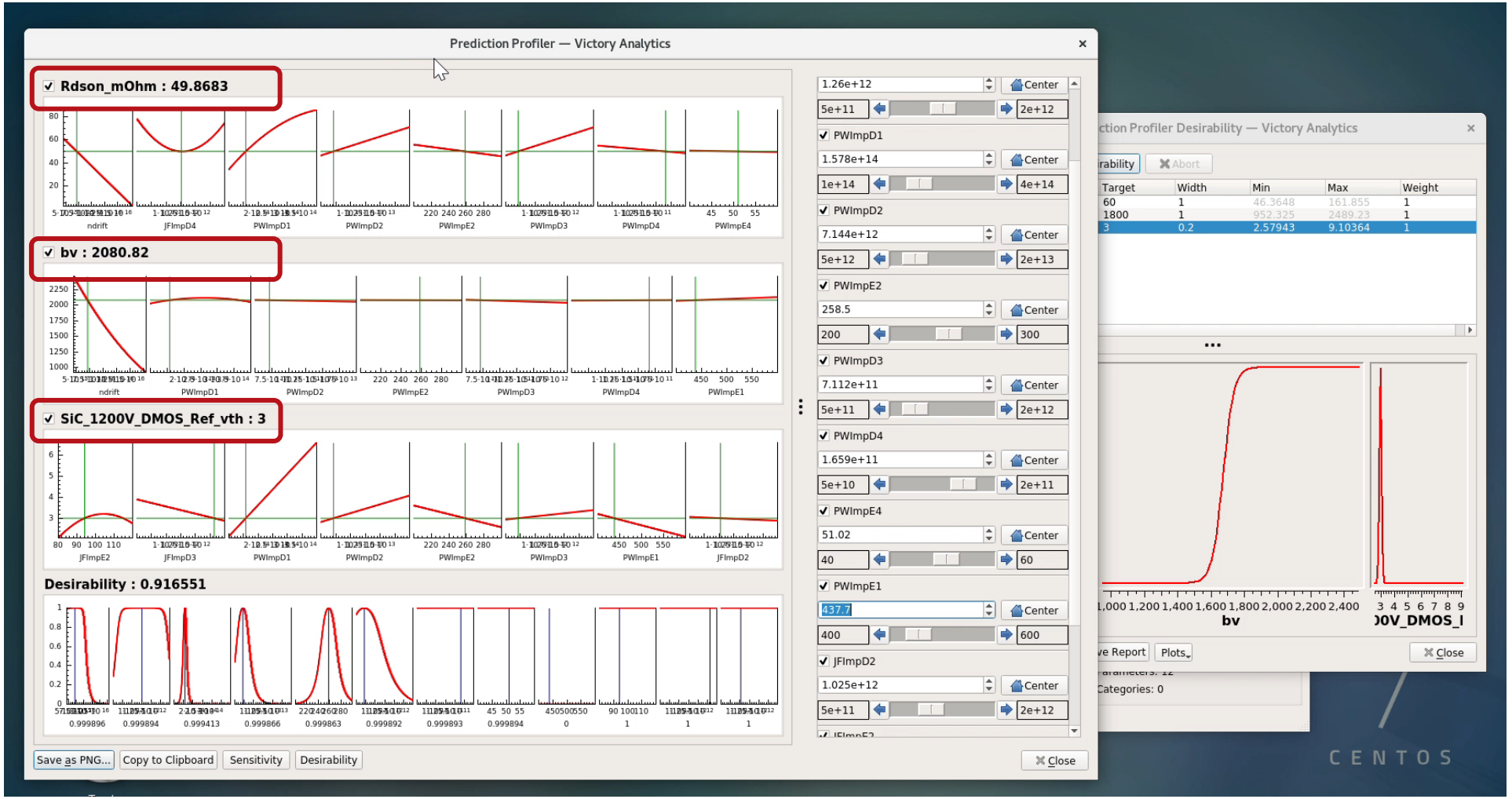
Optimization On Targets

Build ML Model and Home-in on the Targets – Setting Targets and Rubberbanding



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Exploring Other Challenges With FTCO™

How Robust Is My Design To Lot-to-Lot Variation?

Engineer Objective

- Perform Process Capability Analysis
- Improve Robustness to Process Variation

Inputs to the Digital Twin

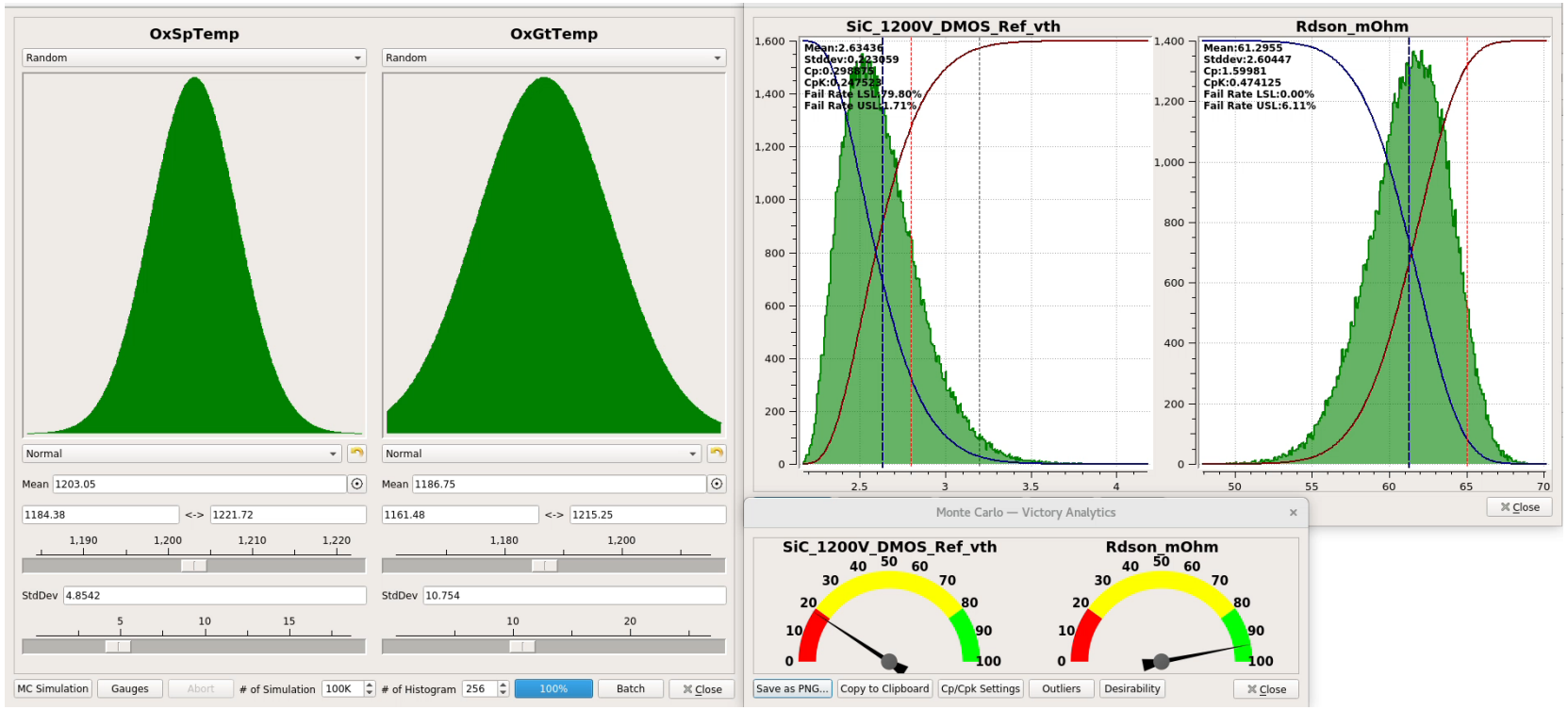
- Process Parameters:
  - Lot-to-lot variation in oxide thickness

Output from Digital Twin

- Process Metrics: Epi-thickness, **Oxide Thicknesses**, Doping Profiles
- Device Metrics: Vth, RdsOn, BV

Goals

- Perform Monte Carlo Analysis
- Cp/Cpk Analysis



The FTCO™ generated Digital Twin allows us to analyze how process variation can affect yield.

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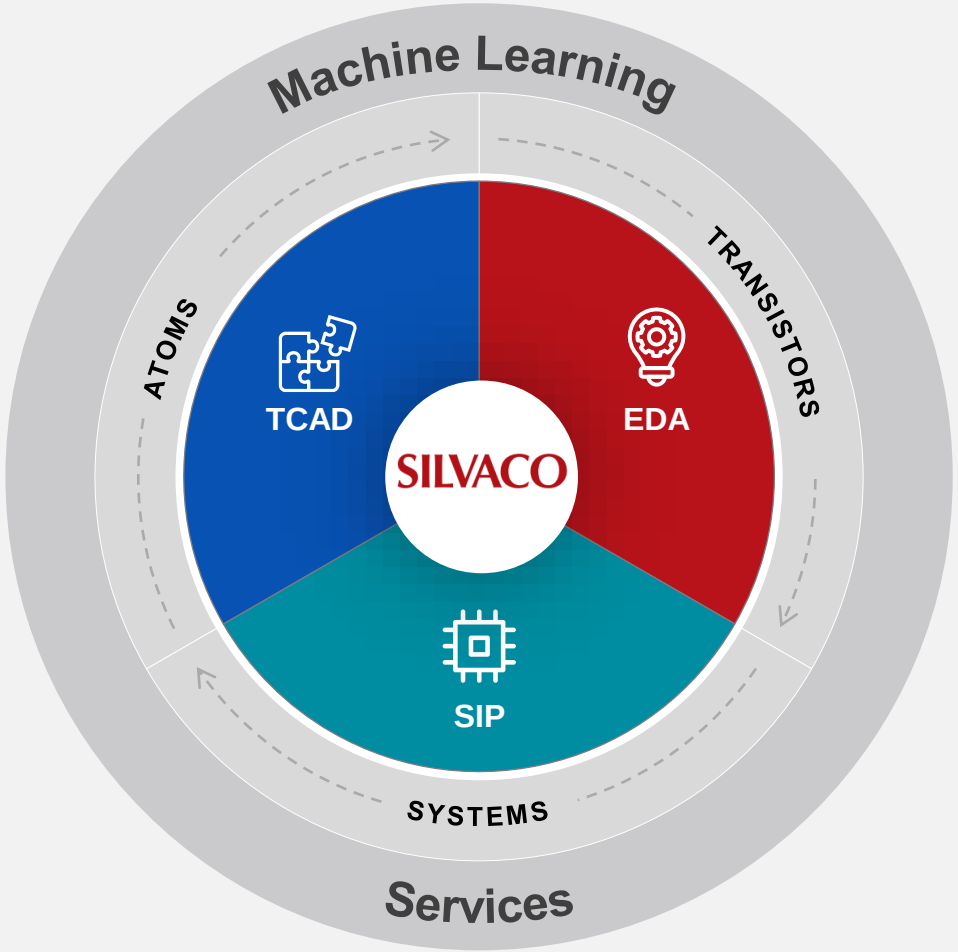

Summary

- FTCO™ generated Digital Twins are enabled by adding machine learning services on top of our core services
- Digital Twins enable optimization of manufacturing processes, reduced costs and increased yields
- Our tools enable the understanding of new technologies
- Our expertise spans from Atomistic to System-level IP
- Our solutions have been used in production flows for the past four decades
- Our agile R&D teams enable and adapt to your needs
- We are driven by your success